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14. ABSTRACT
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Flexible electronics have many developing applications, such as liquid crystal displays (LCDs), organic light-emitting diodes (OLEDs), flex-circuits with connectors and flexible solar cells. Transparent amorphous oxide semiconductors (TAOSs) are the likely candidates to form the active layer of the pixel-driven thin film transistors (TFTs) due to their good uniformity, excellent electrical and optical properties, and compatibility with low temperature deposition. The excellent properties of indium gallium zinc oxide (IGZO) make it the prime candidate; however, the increase in demand of indium has driven up the price. Hence, cheaper substitutes for indium which can produce TAOS TFTs suitable for plastic substrates with comparable characteristics are desired. The focus of this work is on the investigation of the effect of radio frequency (RF) sputtered deposition parameters on the gallium tin zinc oxide (GSZO) based thin film transistor performance and stability. The compositional, optical and morphological properties of the films were examined using x-ray spectroscopy, x-ray reflectivity, Rutherford backscattering and optical absorption techniques. The TFTs were characterized using room temperature current - voltage and capacitance-voltage characteristics and their optical and electrical stability were examined. It was found that that the TFT performance for the GSZO channel deposition and annealing temperature below 140 °C are sensitive to the deposition parameters. The oxygen deficient deposited films led to porous films, with high electron trap density, shallow oxygen vacancies and Zn interstitial states. The oxygen rich ambient deposition on the other hand led to smooth surface and interfaces with dense films with Sn in the desired Sn 4+ state. However, these are dominated by deep filled states. The electrical and optical stability was found to be sensitive to these deposition conditions. The overall performance as well as stability can be significantly improved with marginal increase in the annealing and deposition temperature. In addition, this work includes the process of successful fabrication of bottom-gate TFTs on polyethylene naphthalate (PEN) substrate. TFTs on PEN showed drain current ~10-7 A, ‘on’ voltage ~0 V, subthreshold swing ~0.7 V/decade, an on/off current ratio ~105 and a field-effect mobility ~0.7 cm2/V•s. Our work thus shows that overall GSZO has a very good potential to replace IGZO.

A Study of GSZO TFTs for Fabrication on Plastic Substrates

Robert Alston

North Carolina A&T State University

A dissertation submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Department: Electrical and Computer Engineering

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Dedication

It takes a village to raise a child.-Unknown

The words inked onto the pages of the book you hold were typed by a community of altruistic individuals through the hands of one man. I, Robert Antoine Alston, would not be where I am today if it had not been for this selfless community. No one person is greater than the rest for we are all equal in the eyes of Jesus.

Be strong and have courage, banish fear and doubt for the Lord you God is with you everywhere you go. – Joshua 1:9

It is not possible for me to type this paragraph without becoming teary for I am faced with the dilemma of putting together the correct words to dedicate this book to the Most High. Just as the drummer boy had nothing more to present before the king but his drum, I have nothing more to present to God than the words within this book and my life as gifts for guiding my life the way you have. I pray that you use this book and my life to bless many others as you blessed me.

May you always be intoxicated with her love. –Proverbs 5:19c

I would also like to dedicate this to the love of my life. The dream of earning a Ph.D. does not come close to the reality that I am blessed to wake up to my beautiful wife every morning. Through sacrifice, she has strained to keep her eyelids close every night since 2005 as I studied late at night, whether we were in the school library, computer labs or dorm room. I am forever in debt to her for revealing to me what it means to truly love someone.

Honour thy father and thy mother: that thy days may be long upon the land which the LORD thy God giveth thee. – Exodus 20:12

After years of the pavement thrashing a force equal and opposite to her shoes, my mother now fights arthritis in almost every joint in her legs, shoulders and hands. She did this so that her 5 children may have clothes on their backs, a roof over their heads and food in their bellies. To this we are grateful and in debt. I would also like to dedicate this book to my loving father who convinced me not to take the first job offer and instead pursue graduate school. This showed me that he not only has a big heart but a big brain also. I am also thankful for 4 of the best brothers I ever could've had. Thank you James Ray Cole, Fernando Odzza Alston Jr., Donte' Ronnel Alston and Deangelo Arnez Alston for protecting me from harm and being my best friends.

Our guardian angels are closer to us than anything except the love of God. - Eileen Elias Freeman

There are no words to describe what Ms. Hazel and the Broadnax family has sacrificed for me. Like a stray dog with a dream of a better life I stumbled upon Ms. Hazel. She then took me into her home, fed me, clothed me and finished the work of my mother by teaching me how to be a man. When I needed a friend she became that friend. When I needed money for college she was there to help me. When I needed advice on what to do next she guided me and I cannot thank her and the Broadnax family enough. I will honor you by doing the same for others.

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μ	Mobility
Ar	Argon
Au	Gold
CB	Conduction band
CBM	Conduction band minimum
C_{ox}	Oxide capacitance
D_{it}	Density of interface traps
DOS	Density of states
E_C	Conduction band energy
ET	Elevated temperature
Ga	Gallium
GSZO	Gallium tin zinc oxide
GZO	Gallium zinc oxide
HMDS	Hexamethyldisilazane
I_D	Drain current
IGZO	Indium Gallium Zinc Oxide
In	Indium
I_{OFF}	Off current
$I_{ON/OFF}$	On/off current ratio
IZO	Indium zinc oxide
M-OH	Metal hydroxides

N_2	Nitrogen gas
O	oxygen
O_2	Oxygen Gas
PR	Photoresist
q	charge
RF	Radio Frequency
RT	Room Temperature
SCCM	Standard cubic centimeter per minute
Si	Silicon
SiO_2	Silicon Dioxide
Sn	Tin
SS	Subthreshold swing
SZO	Tin zinc oxide
TAO	Transparent Amorphous Oxide
TCE	Trichloroethylene
TCO	Transparent conducting oxide
Ti	Titanium
TFT	Thin Film Transistor
UV	Ultra violet
V_G	Gate voltage
V_{DS}	Drain to source voltage
V_o	Oxygen vacancies
V_T	Threshold voltage

W/L	Width / Length ratio
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction
Zn	Zinc
ZnO	Zinc Oxide

Abstract

Flexible electronics have many developing applications, such as liquid crystal displays (LCDs), organic light-emitting diodes (OLEDs), flex-circuits with connectors and flexible solar cells. Transparent amorphous oxide semiconductors (TAOSs) are the likely candidates to form the active layer of the pixel-driven thin film transistors (TFTs) due to their good uniformity, excellent electrical and optical properties, and compatibility with low temperature deposition. The excellent properties of indium gallium zinc oxide (IGZO) make it the prime candidate; however, the increase in demand of indium has driven up the price. Hence, cheaper substitutes for indium which can produce TAOS TFTs suitable for plastic substrates with comparable characteristics are desired. The focus of this work is on the investigation of the effect of radio frequency (RF) sputtered deposition parameters on the gallium tin zinc oxide (GSZO) based thin film transistor performance and stability. The compositional, optical and morphological properties of the films were examined using x-ray spectroscopy, x-ray reflectivity, Rutherford backscattering and optical absorption techniques. The TFTs were characterized using room temperature current -voltage and capacitance-voltage characteristics and their optical and electrical stability were examined. It was found that that the TFT performance for the GSZO channel deposition and annealing temperature below 140 °C are sensitive to the deposition parameters. The oxygen deficient deposited films led to porous films, with high electron trap density, shallow oxygen vacancies and Zn interstitial states. The oxygen rich ambient deposition on the other hand led to smooth surface and interfaces with dense films with Sn in the desired Sn^{4+} state. However, these are dominated by deep filled states. The electrical and optical stability was found to be sensitive to these deposition conditions. The overall performance as well as stability can be significantly improved with marginal increase in the annealing and deposition

temperature. In addition, this work includes the process of successful fabrication of bottom-gate TFTs on polyethylene naphthalate (PEN) substrate. TFTs on PEN showed drain current ~10^{-7} A, 'on' voltage ~0 V, subthreshold swing ~0.7 V/decade, an on/off current ratio ~10^5 and a field-effect mobility ~0.7 $cm^2/V \cdot s$. Our work thus shows that overall GSZO has a very good potential to replace IGZO.

CHAPTER 1

Introduction

1.1 Motivation

Tremendous efforts have been made in the development of amorphous oxide semiconductor thin film transistors (AOS TFTs) device research, resulting in possible applications such as flexible display applications and switching transistors in active matrix liquid crystal displays (AMLCD). Promising materials are amorphous ZnO based alloys exhibiting wide band gap (3.2 eV), such as indium gallium zinc oxide (IGZO), zinc tin oxide (ZSO) and gallium tin zinc oxide (GSZO). The major advantage of oxide semiconductor materials is that they can be deposited using conventional semiconductor process methods such as sputtering at room temperature, and their amorphous structure enables the realization of uniform device properties over large areas. Due to large overlapping s-orbitals from heavy metal cations, much higher electrical performance can be achieved using n-type oxide semiconductors with practical field effect mobility (μ_{FE}) values exceeding 5 $cm^2/V \cdot s$. These are less sensitive to light and exhibit good uniformity and high quality after being deposited near room temperature. Because of such remarkable characteristics, AOS TFTs are excellent candidate switching elements for large area (>70 in.), ultra definition (UD, 4k x 2k), and fast frame (>240 Hz) AMLCD panels [1].

Amongst these, IGZO appears to be more promising due to its benefits of Ga incorporation which aids in stability and In incorporation that improves device field-effect mobility (μ_{FE}) >10 $cm^2/V \cdot s$ [2]. However, due to the high demand and scarcity of In it is an expensive element and thus a replacement material is being researched (Figure 1). The extensively researched electrical properties of a-IGZO have set a high standard for replacement

alloys. In replacing In, Sn appears to be promising since Sn^{4+} has the same electronic configuration, $[Kr](4d)^{10}(5s)^{0}$, to In^{3+} and is more abundant [3, 4].

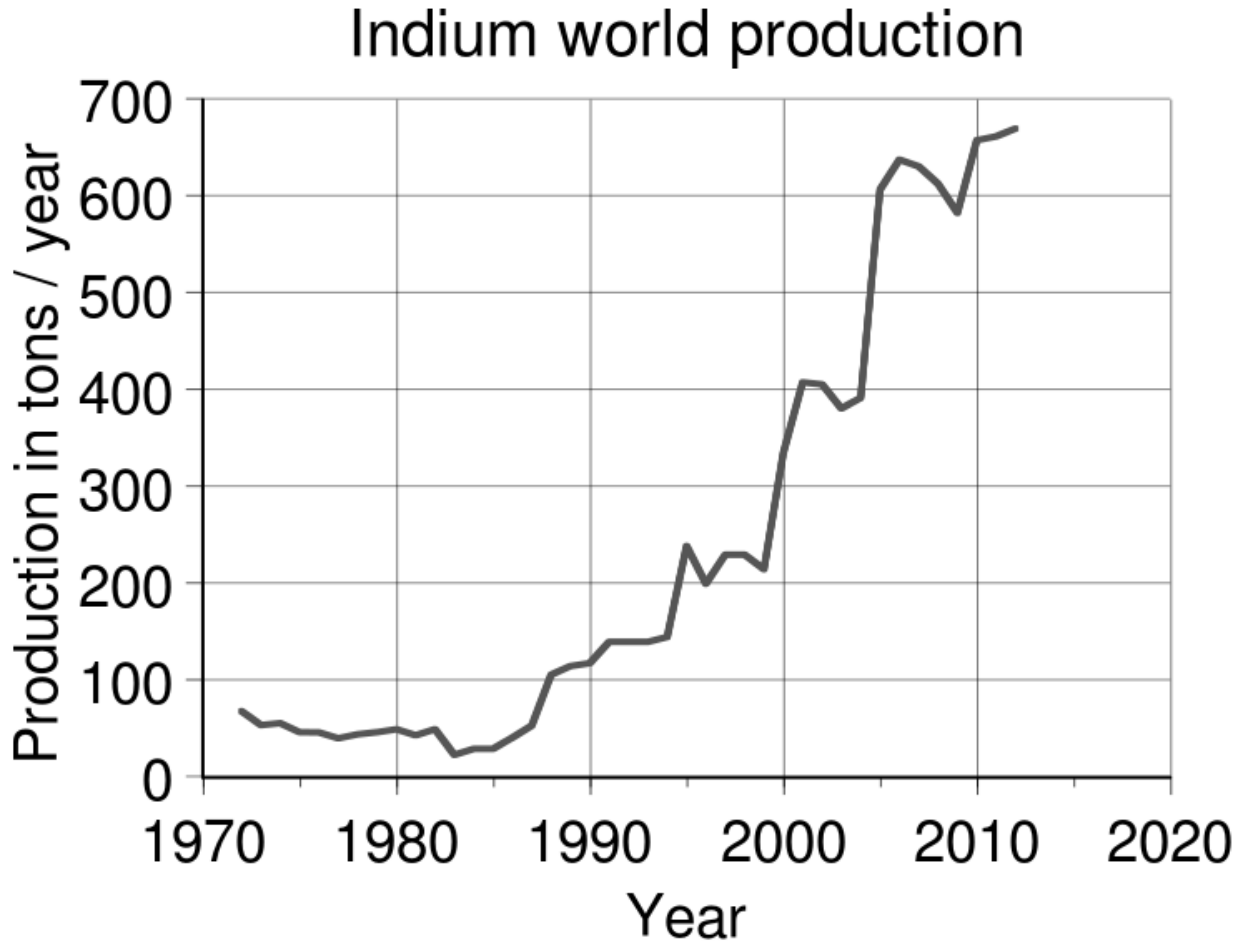

Figure 1 Indium world production [5]

1.2 Background

In this section the historical background of amorphous oxide TFTs, its corresponding challenges as well as experimental progress will be presented. Before the incorporation of amorphous oxide TFTs in industrial applications, amorphous silicon TFTs dominated the display field as semiconductor device of choice. A common application which incorporates a-Si TFTs is the liquid crystal display which is the preferred display in portable computers. In addition to PCs, LCDs are commonly used in mobile phones, digital cameras, camcorders, personal digital

assistants (PDAs), game machines, TVs, global position systems (GPSs), industry and mechanical instruments transportation and military systems [6].

What makes AOS design unique is the selection of cations from the portion of the periodic table shown in Figure 2 since such cations possess conduction bands derived from large ionic-radius, spherically symmetric 4s, 5s or 6s electron orbitals [7]. These orbitals lead to a high degree of wave-function overlap, electron delocalization and relatively high electron mobility, independent of whether the microstructure is crystalline or amorphous. Specifying cations from Figure 2 combined in multi-component systems confuse the lattice as to which structure type to adopt thus tending to an amorphous structure. Elements colored red should be avoided because of their toxicity (As, Cd, Hg, Tl, Pb) while those colored brown use best used for p-type semiconductors (Cu, Ag, Au). The elements colored orange are less attractive due to high cost (Ge, Ag, Au), while elements colored blue are most commonly used in AOS design (Zn, Ga, In, Sn). Elements in black have not yet been proven in literature to be useful in AOS systems (Sb, Bi). Elements Ga and In has cost concerns while In is sometimes classified as toxic. Therefore it is very clear that Zn and Sn are the two most attractive AOS cation choices from the perspective of abundance, cost, world-wide production and toxicity.

11	12	13	14	15	
29 Cu 63.54	30 Zn 65.37	31 Ga 69.72	32 Ge 72.59	33 As 74.92	4
47 Ag 107.87	48 Cd 112.40	49 In 114.82	50 Sn 118.69	51 Sb 121.75	5
79 Au 196.97	80 Hg 200.59	81 Tl 204.37	82 Pb 207.19	83 Bi 208.98	6

Figure 2 Portion of the periodic table for selecting amorphous oxide semiconductor cations. Color coding: Blue=most common cations employed in AOS design, red=toxic, brown=p-type cations, orange=high cost cations, black=largely uninvestigated.

1.2.1 AOS Films and TFTs Low temperature poly-silicon (LTPS) was universally regarded as the successor to amorphous silicon (a-Si) when its mobility performance was deemed inadequate for emerging display applications. Table 1 shows device performance with semiconductor material candidates as the active layer. Switching speed is a measure of required voltage to increase the drain current an order of magnitude and the leakage current is considered the current flow when the device is 'off'. In terms of mobility performance, LTPS is shown to be superior to a-Si and also has superior stability characteristics. Finally, the availability of CMOS using LTPS means that row and column drivers or other peripheral circuits can be integrated onto the glass substrate, an attractive option. However the emergence of AOSs bring exciting possibilities even though it does not have as high an electron mobility as LTPS because it is amorphous. Being amorphous it possesses the same inherent manufacturing/scaling/cost advantages as a-Si involving threshold voltage (V_T), mobility uniformity and process simplicity. Three useful attributes of AOSs include the absence of a Staebler-Wronski-like instability mechanism that limits a-Si, the ease of moving the Fermi energy into extended states and the

high mobility [8]. TAOs have a direct overlap among the neighboring metal orbitals (Figure Figure *3*) that produce an optimal carrier transport path than that of covalent semiconductors in the amorphous state, such as a-Si. The semiconductor ZnO gained incredible interest due in part to its large exciton binding energy (60 meV) which could lead to lasing action based on exciton recombination even above room temperature. Though it is not new to semiconductor research with studies dating back to 1935 and light-emitting diodes (LEDs) in 1967, interest has increased due to its quality when used in TFTs after being doped with transition metals.

Table 1

Comparison of common semiconductor materials used as active layer in TFTs

TFT Properties	**Oxide Semiconductors**	Amorphous Si	Low-T Poly-Si	Organic Semiconductors
Carrier Mobility [$cm^2V^{-1}s^{-1}$]	**1-100**	1 (max)	50-100	0.1-10
Switching [$Vdec^{-1}$]	**0.1-0.6**	0.4-0.5	0.2-0.3	0.1-10
Leakage Current [A]	**$1x10^{-13}$**	$1x10^{-12}$	$1x10^{-12}$	$1x10^{-12}$
Manufacturing Cost	**Low**	Low	High	Low
Long Term TFT Reliability	**High**	Low	High	Low in air

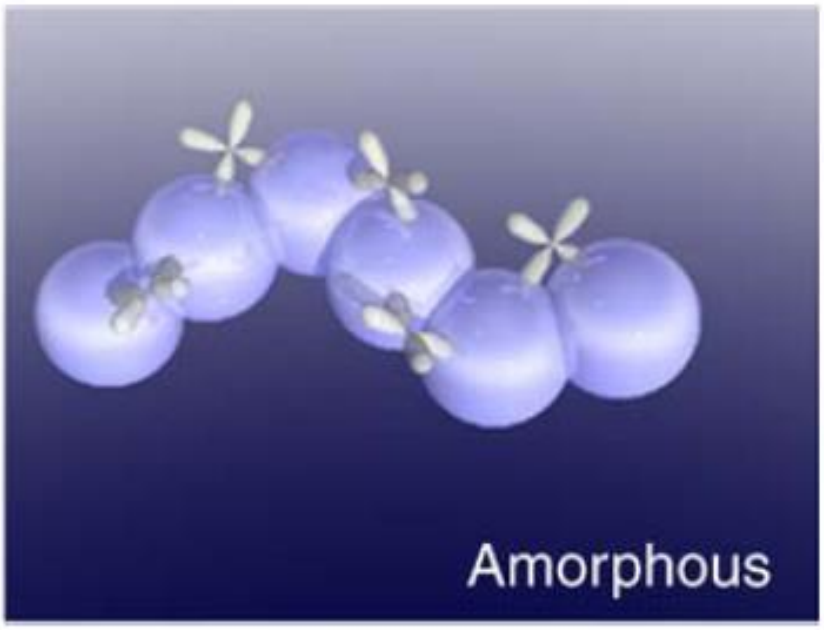

Figure 3 Carrier transport paths for TAOSs composed of post transition metal cations [9]

A common doped-ZnO semiconductor used in TFT applications is indium-gallium-zinc-oxide (IGZO). Due to its low cost, good uniformity, large Hall mobility and excellent TFT characteristics, IGZO applications has increased recently with such being solar cells and active matrix flat-panel displays [10]. However a glaring problem with the incorporation of indium in display applications is it rarity and thus price. Indium is a by-product of mining ores for other metals such as zinc, copper, lead and tin thus it is estimated that there is more than 1000 times zinc in the earth's crust than indium [11]. Thus the replacement of indium is vital for AOS TFT applications. Tin-based AOSs such as Sn-Zn-O and Ga-Sn-Zn-O (GSZO) are promising substitutes because a Sn^{4+} ion has the same electronic configuration ,$[Kr]5s^0$, as that of In^{3+} which meets the criterion for high mobility TAOS materials [12].

AOS TFTs are now being commercialized for AMLCD backplane applications. They also appear to be well positioned for other flat-panel display applications such as AMOLED applications, electrophoretic displays and transparent displays. Flexible LCDs for electronics

have already been implemented using amorphous-indium gallium zinc oxide (a-IGZO) semiconductor thin film transistors (TFTs) by large companies such as Samsung Electronics, Sharp, Fujitsu, LG Electronics and Apple [13-17].

1.3 Objectives

The focus of our work is to improve the electrical performance of TAOS TFTs while substituting In with Sn in preparation for TFTs on plastic substrates. The leading candidate in amorphous oxide semiconductors (AOSs) in TFT applications is indium gallium zinc oxide (IGZO). With a large mobility, low sub-threshold swing (SS), good uniformity and low-temperature processing, IGZO's usage in display technology has already begun [18]. Indium however is an economical and industrial problem due to its scarcity making it expensive to be used in mass production items. Strong motivation from this research is the ability to produce TFTs comparable to IGZO TFTs without the use of indium. An element that is a candidate for replacing In due to its comparable electronic configuration is Sn. Very little work has been done on the production of GSZO TFTs though it has been demonstrated [12, 19] that it is a possible alternate material system of interest. A common problem associated with ZnO based amorphous oxides is the high level of carrier traps associated with oxygen vacancies and other point defects formed in its hexagonal wurtzite structure as well as semiconductor/insulator interface. Identification and controllability of these traps are needed to overcome this problem. Finally this research will focus on transferring GSZO TFTs from a non-transparent Si substrate to a plastic substrate made of polyethylene naphthalate (PEN).

This research work addresses three major problems:

1. A common problem associated with ZnO based amorphous oxides is the high level of carrier traps due to various point defects formed in its hexagonal wurtzite structure and at

the interface between the oxide and channel. Identification and controllability of these traps are the major problems associated in improving the performance of the TFT. In this research work we have carried out a systematic and detailed investigation analyzing the effects of TFT fabrication parameters on formation and controllability of such defects and interface traps.

2. It has been reported that illumination stability (involving a threshold voltage shift to negative voltages) is the greatest technical challenge facing AOS TFT technology [20]. A systematic optical stress has been performed using 3 different wavelengths for different durations to examine the density of traps within the band-gap of the GSZO film. Along with optical stress, negative bias illumination stress (NBIS) involving light at 550 nm shone onto the semiconductor while applying a negative bias to the gate has been conducted as well as the commonly used positive bias stress (PBS) and negative bias stress (NBS) tests were conducted.
3. Finally this research will focus on transferring GSZO TFTs from a non-transparent Si substrate to a plastic substrate made of polyethylene naphthalate (PEN).

Details of achieving the above specific objectives of the research are as follows:

- Fabricate TFTs with GSZO active layers, replacing In with Sn: This was accomplished by RF-sputtering of GSZO thin films onto thermally oxidized SiO_2 on n^+ Si substrates. Photolithographic processes were used to fabricate bottom-gate GSZO TFTs and electron beam (e-beam) methods were used to form Al S/D contacts.
- Improve GSZO device performance while maintaining process temperatures below 140 °C: All annealing and deposition temperatures were kept at 140 °C, unless intended to

analyze effect of high annealing temperatures. Annealing processes were done in air while sputtering processes were done in 10:1 Ar/O_2 plasma.

- Further improve GSZO device performance by varying growth and process conditions: Process parameters such as deposition pressure, deposition temperature, annealing duration, annealing temperature as well as channel thickness were varied to further improve the performance of the GSZO devices.
- Correlate the effects of various growth and processing parameters on the nature and location of the defect and trap density: Insight into the trap density, I-V, hysteresis, C-V and stability measurements were taken. C-V measurements were taken at frequencies varying from 250 Hz to 1 MHz, photo-stability tests were done with different wavelengths of illumination and electrical stability under both positive and negative bias over a prolonged period were used to get an insight the distribution of the states in the bandgap and its effects on the TFT performance.
- Fabricate GSZO TFTs on a plastic substrate: GSZO TFTs were fabricated on PEN to using a bottom gate structure with Mo gate contact and Al S/D contacts. The gate oxide was deposited through PECVD method by Research Triangle Institute (RTI) Int'l while the GSZO film was deposited in-house.

1.4 Outline of the Dissertation

This dissertation consists of seven chapters which are listed below in an outline of this study.

Chapter 1 discusses the background, motivation and objectives behind this work. The motivation discusses the high cost of In and the importance of finding a replacement metal with similar electronic configuration to replace it. The background gives a brief introduction to AOS

TFTs, definition of various parameters used in TFTs to describe its performance, history and various applications. Lastly the objectives of this work and the steps taken to achieve the goals are described.

Chapters 2 reviews the published literature related to TAOS TFTs. Amongst published literature lies a description of various parameters that were varied to investigate the performance of TAOS TFT devices and to examine the properties of the material. The chapter is divided into 2 sections focused on the popularly researched IGZO TFTs as well as GSZO TFTs. Device performances in terms of I-V and C-V results and their electrical and optical stability are presented.

In Chapter 3 a description of the experimental set ups is given. This chapter includes SiO_2 oxidation, RF sputter deposition, photolithography process, metal deposition and film annealing. Also discussed in detail are the TFT structures used on Si and on PEN substrates.

Chapter 4 presents the material and device characterizations used in this work. Various techniques were used namely x-ray photoelectron spectroscopy (XPS) for elemental composition, atomic force microscopy (AFM) and x-ray reflectivity (XRR) for surface morphology, Rutherford backscattering spectrometry (RBS) for more accurate atomic concentration and optical absorption measurements for calculating film transparency and material bandgap. I-V and C-V measurements used in determining the electrical characteristics of TFTs and the set up used for electrical stability and optical stability are described.

Chapter 5 discusses the analysis of GSZO films and the electrical performance of GSZO TFTs fabricated under various process. Effects of annealing temperature reduction from 250 °C to 140 °C for 1 hour, increase in deposition temperature from 50°C to 100 °C, variation in annealing duration at 140 °C and the variation in GSZO film thickness on the device

performance were investigated. The devices fabricated on PEN are also presented. Characterizations such as XRR, XPS, RBS, I-V and C-V were used to analyze the films and devices and results are presented and described in this chapter.

Chapter 6 discusses the characterizations described above on GSZO films and devices with GSZO active layer deposited at various deposition pressures. Characterizations listed above, PBS, NBS, NBIS and optical stress tests were conducted to investigate the location of trap densities at energy levels.

Chapter 7 discusses the results and analysis from chapters 5 and 6 with plausible causes. Results from each of the characterization technique is presented and analyzed. Finally these were used to provide a greater insight into the interface engineering and its impact on GSZO device performance. This leads to the potential of Sn substituting In for future AOS TFT fabrication.

Chapter 8 presents an overview of the findings of this research as well as possible future work to improve device performance.

CHAPTER 2

Literature Review

2.1 Introduction

This literature review gives an overview on the recent and past relevant published works on the AOS TFTs. There are many published papers in this work and more than 5 review articles on AOS TFTs. Hence we have focused in this chapter on a very selective published work relevant to this dissertation. As mentioned in chapter 1, due to high cost associated with scarcity, the investigation of this research is in the replacement of In with Sn [21]. Candidate materials for high mobility TAOS TFTs are required to have heavy metal cations with $(n-1)d^{10}ns^0$ electronic configurations (where the principal quantum number $n \geq 5$) as a major constituent. Both In^{3+} and Sn^{4+} share the same electronic configuration $[Kr](4d)^{10}(5s)^0$ [22] hence Sn is a good choice for replacing In.

The following literature review displays some reported literature on the effects of deposition and annealing conditions on AOS TFTs. Investigations of the effects of different deposition and annealing temperatures, electrical and optical stability, deposition pressure and channel thickness are presented as well as AOS TFTs reported on plastic substrates and applications. A comparison of IGZO, GSZO and ZSO TFTs is shown.

2.2 Deposition Temperature

2.2.1 IGZO Jie et al. [23] analyzed the effect of deposition temperature on the performance of sputtered a-IGZO TFTs. The deposition temperature was controlled by heating the substrate and was intentionally set to room temperature (RT), 150 °C, 200 °C, 250 °C and 300 °C respectively. Finally the TFTs were annealed in air at temperatures varied from 150 °C to 350 °C to find the optimized annealing temperature for the devices with active layers deposited

at different temperatures. It was discovered that μ_{FE} reached maximum at deposition temperature of 150 °C while the room-temperature fabricated device showed the best SS and I_{OFF}. XPS characterization results revealed that deposition temperature affects the atomic ratio and O1s spectra. Based on results it was determined that trap states at front channel interface rather than bulk layer properties are mainly responsible for the variations of μ_{FE} and SS with IGZO deposition temperature.

2.2.2 GSZO Fortunato et al. [11] investigated the performances of TFTs with the replacement of Indium with Tin. The GSZO film was deposited by RF magnetron co-sputtering. The targets used were GZO and Sn. Two sets of TFTs were analyzed and compared, one set with its channel layer deposited at room temperature and annealed at 200, 250, and 300 °C respectively, and the other set with its channel layer deposited at 150 °C and annealed at 200, 250, and 300 °C. Room temperature TFTs did not begin to operate until post annealed equal to and greater than 250 °C. TFTs with channel layers deposited at an elevated temperature were not stable until annealed to 200 °C. Saturation mobilities increased with increasing annealing temperatures. After post annealing at 300 °C, room temperature TFTs exhibited a saturation mobility of 18.1 $cm^2/V \cdot s$, and the elevated temperature TFT exhibited a saturation mobility of 24.6 $cm^2/V \cdot s$. This improvement with annealing temperature is attributed to modification of the semiconductor/insulator interface with temperature and/or to improved local atomic rearrangement. It was also observed that post annealing did not alter the amorphous state of the TFTs fabricated.

Moon et al. [24] evaluated the combined effects of deposition and annealing temperatures on the micro-structure of IGZO films and its corresponding TFT performance. Four sets of IGZO films were prepared, one deposited on an unheated substrate and others on a substrate heated to

100 °C, 200 °C and 250 °C. The samples were then annealed at different temperatures (100 °C, 200 °C, 300 °C and 400 °C) in oxygen ambient for 1 hour in a furnace. To examine the microstructure of the heated films, high-resolution transmission electron microscopy (HR-TEM) and energy-filtered selected area electron diffraction (EF-SAED) was combined following a methodology widely adopted in the field of bulk metallic glasses. High resolution electron micrographs showed an amorphous structure for the RT and 100 °C films however an increase in atomic clustering appeared for the 200 °C and 250 °C films. EF-SAED analysis supported the move of the IGZO films towards crystallinity with increasing substrate temperature during the deposition. This suggested that substrate heating facilitates atomic ordering by allowing adsorbed atoms to diffuse more readily and construct an atomic structure with enhance atomic order.

2.2.3 ZSO There has been no published literature reporting on the effects of annealing temperature on ZSO TFTs.

2.3 Annealing Temperature

2.3.1 IGZO Oh et al. [25] presented the effects of hydrogenation on the surface characteristics of a-IGZO TFTs by applying a high pressure hydrogen annealing (HPHA) process under 5-atm pressure at different temperatures of 260 °C, 270 °C and 280 °C. HPHA effectively increased the carrier concentration and Hall mobility (~10^9 cm^{-3} and ~6.4 $cm^2/V{\cdot}s$). The HPHA TFTs of 260 °C showed enhanced electrical characteristics, leading to a μ_{SAT} of 7.4 $cm^2/V{\cdot}s$, an SS of 0.37 V/dec, a V_T of 2.2 V and an $I_{ON/OFF}$ of 2x10^6. The HPHA-IGZO films exhibit smoother surfaces as compared to as-grown films. HPHA was found to be an efficient way to control the carrier concentration in the IGZO film by changing the annealing temperature. The carrier concentration could be modulated up to 100 times without severely deteriorating the carrier mobility simply by changing the process temperature. The process temperature was found

to be much lower than the required process temperature of other reported hydrogenation methods which is due to a high hydrogen incorporation rate where the hydrogen gases had higher solubility and diffusivity with hydrogen partial pressure.

2.3.2 GSZO Kim et al. [26] investigated the effect of post-annealing on the electrical properties of a-GSZO films with different Ga contents. The films were deposited at room temperature by sputtering and annealed in air for 1 hour. It was found that the doping with Ga, which acts as the carrier suppressor, contributes to the thermal stability of the characteristic properties of a-GSZO thin films. The film with a small amount of Ga showed significant variations in carrier concentration according to the annealing temperature. After annealing at 400 °C, the enrichment of Zn cations in the surface region resulted in considerable changes in chemical bonding states and consequently, the carrier concentration decreased by 2 orders of magnitude for the low Ga-doped GSZO film.

Ogo et al. [12] investigated the performance of GSZO TFTs as deposited, and post annealed up to 600 °C. The GSZO films were deposited by room temperature pulsed laser deposition (PLD), and the TFTs had a bottom gate configuration. It was observed that GSZO films are stable up to 600 °C post annealing and afterward the films are no longer amorphous because GSZO does not have a stable crystal at thermal equilibrium. AFM images indicate a small root mean square roughness R_{rms} less than 0.3 nm for the 600 °C annealed films. The threshold voltages increased from -7.7 to 6.8 V as annealing temperatures increased from 200 °C -600 °C. Saturation mobilities and subthreshold voltages increase with increasing annealing temperatures with a saturation mobility of 2 $cm^2/V{\cdot}s$ and a subthreshold voltage of 5 V/dec. All TFTs exhibited a clockwise hysteresis greater than 2 V revealing that electron traps existed within the gate dielectrics. It was found that the higher-quality annealed a-GSZO film exhibits an

Urbach tail region below the Tauc region. The as-deposited a-GSZO film had the strongest sub-gap absorptions which would come from defect states formed by incorporation of Sn ions.

Hosono et al. [22] compared the transport properties of a-IGZO and a-GSZO films and TFTs to extract the effects of constituent metal cations. Comparison of the TFT performances between the a-IGZO and a-GSZO channels revealed that In-based system has much better performances when the device is fabricated without intentional annealing. Much stronger absorption tail was seen for the as-deposited a-GSZO thin films, attributed to the formation of a low valence state, Sn^{2+}, and relevant defect states located near the CBM deteriorate the TFT performances.

2.3.3 ZSO Chiang et al. [27] reported on ZSO TFTs annealed at 300 °C and 600 °C. The effects of air annealing on the electrical performance of the devices are examined. V_{ON} shifted between 5 V and 15 V and μ_{FE} varied between 5 $cm^2/V{\cdot}s$ and 15 $cm^2/V{\cdot}s$ while sustaining an $I_{ON/OFF}$ of 10^7. ZSO device performance showed little variations between devices with channel layers of different stoichiometry.

2.4 Electrical and Optical Stability

2.4.1 IGZO Lee et al. [28] investigated the effects various gate dielectrics on the stability of the threshold voltage. Gate dielectrics SiN_x and SiO_x are the commonly used gate dielectrics with AOS IGZO TFTs. Inverted and staggered TFTs were produced on Polyimide (PI) films. The thickness of the gate dielectrics were 200nm, and were grown by plasma enhanced chemical vapor deposition (PECVD) at elevated temperature of 150 °C and 350 °C. TFTs with the SiN_x gate insulator grown at 150 °C exhibited a subthreshold gate swing of 1.1V/decade, an $I_{ON/OFF}$ greater than 10^8, and a field effect mobility of 8.1 cm^2 /V·s. The threshold voltage shifted in the positive direction with the SiN_x gate dielectric insinuating that

V_{TH} is largely determined by the density of charge traps within the gate dielectrics. By optimizing the gate dielectric, charge trap concentration induced by hydrogen atoms decreases which increases the performance of a-IGZO TFTs.

Park et al. [29] examined the effect of oxygen high pressure annealing on IZO TFTs with a high-quality passivation layer to improve the photo-bias stability. The channel layer was encapsulated by a high-quality Al_2O_3 film to avoid adverse ambient interactions and further enhance μ_{FE}. The Al_2O_3 passivation layer thickness was ~15 nm and the O_2 HPA annealing was carried out at 6 and 9 atm. for 1 hour at 200 °C. NBIS-induced V_{TH} shift for the O_2 HPA-treated IZO TFTs was reduced from -3.7 V to -0.5 V, whereas the μ_{FE} and $I_{ON/OFF}$ ratio values had not deteriorated. This NBIS-induced negative V_{TH} shift has been explained by the photo-ionization of neutral V_O into a double-charged V_O^{2+} state where a neutral V_O is assumed to be a deep state and electrically inactive.

Kim et al. investigated the change in I-V characteristics of IGZO TFTs under light illumination at different wavelengths. The variations in the interfacial trap density (D_{IT}) were also studied. Bottom-gate a-IGZO TFTs were fabricated with 200 nm SiO_2 gate insulator and highly doped Si for gate electrode. The TFTs were subjected to thermal annealing in air at 300 °C for 1 hour. Typical transfer curves under light illumination at various wavelengths were shown with photo-induced degradation occurring under ultraviolet illumination ($\lambda<400$ nm) due to increased carrier concentration (n_d) in the channel region that comes from band to band transitions. The increase in SS observed under light illumination $\lambda\leq550$ nm was confirmed to be related to the increase in D_{IT} near the CB edge. These states are thought to come from the doubly ionized oxygen vacancies which are generated temporarily under light illumination. The I_{OFF} was

found to increase much faster than the D_{IT} suggesting photo-excited carriers from the VB tail states.

2.4.2 GSZO Jeong et al. [30] generated a novel AOS-TFT with excellent bias-stress stability using solution-processed GSZO layers as the channel. The cause of the resulting stable operation against the gate bias-stress was studied by comparing the TFT characteristics of the GSZO layer with a tin-doped ZnO (ZTO) layer that lacks Ga. By photoluminescence, XPS and electron paramagnetic resonance spectroscopy it was found that the GSZO layer had significantly lower V_O's, which acts as trap sites, than the ZTO film. GSZO TFTs with μ_{SAT} up to 1.2 $cm^2/V \cdot s$, $I_{ON/OFF}$ ~$1x10^6$ and an SS of 1.5 V/dec was observed.

2.4.3 ZSO Chen et al. [3] investigated the effects of bias-induced oxygen adsorption on the electrical characteristic instability of ZSO TFTs in different ambient oxygen partial pressures. Bottom-gate TFTs with 80 nm ZTO films were annealed at 350 °C for 1 hour and 10 V was applied to the gate while the S/D contacts were grounded. It was observed that VT was strongly affected by bias-induced oxygen absorption on the back channel during the stress phase and by the amount of surrounding oxygen molecules during the recovery phase. VT shifted positively with tiny variations in SS and ION for devices stressed in vacuum (10-4 torr) which is generally attributed to electrons trapping in the pre-existing traps located at the interface or in the gate dielectric. These devices recovered within 1000 s which is attributed to the detrapping of previously trapped charges. A stronger shift in VT during the stress phase was observed for devices stressed in vacuum however it recovered to its original characteristics rather quickly in atmospheric ambient.

2.5 Deposition Pressure and Gas Flows

2.5.1 IGZO Aoi et al. [31] investigated the effects of the partial pressure of H_2O during sputtering deposition and the structural and electrical characteristics of the films grown. H_2O was found to be effective in reducing oxygen vacancies thus reducing carrier concentrations. A field effect mobility of 1.4– 3.0 $cm^2/V{\cdot}s$, sub-threshold swing of 1.0–1.6 V/decade and an on–off current ratio 3.9×10^7–1.0×10^8 was observed as the IGZO layer was deposited under an H_2O partial pressure of $1.6–8.6\times10^{-2}$ Pa.

Barquinha et al. [32] investigated the effects of various parameters such as oxygen partial pressure, deposition pressure, target composition, thickness, and annealing temperature have on the electrical properties of IGZO. TFTs with annealing temperatures as low as 150°C produced TAOSs with good switching properties such as V_{ON} close to 0, V_T between −1.0 V and 1.0 V, respectively and low SS = 0.25 V/dec, accompanied by a high μ_{FE} = 51.7 $cm^2/V{\cdot}s$ and on-off ratio of 2 $x10^8$.The chosen IGZO target composition was 1:2:2 deposited with the oxygen partial pressure (P_{O2}) = 1.5 mPa, deposition pressure (P_{dep}) = 0.7 Pa, and channel thickness (d_s) = 40 nm.

Jung et al. [33] investigated the electrical and optical properties of a-IGZO under various processing gas flows. The IGZO thin films were deposited onto glass substrates with a constant processing pressure of 0.13 Pa, and film thicknesses around 50nm. Various gas flows such as Ar, Ar-4% H_2, O_2/Ar+O_2, and O_2/Ar-4% H_2+O_2 at room temperature were used during sputtering processes. All films deposited under O_2/Ar+O_2, and O_2/Ar-4% H_2+O_2 showed optical transmittance above 90%. Films deposited under Ar showed optical transmittance around 90% and films deposited under Ar-4% H_2 revealed a dramatic decrease in transmittance between 40 and 50%. Films deposited under Ar and Ar-4% H_2 resulted in suitable electrical characteristics,

carrier concentration between $10^{18\text{-}19}$ cm^{-3}, a good SS value of 0.04 V/dec, a threshold voltage of 0.34V, and a field effect mobility of 3.6 cm^2 $V^{-1}s^{-1}$.

2.5.2 GSZO There has been no published literature reporting on the effects of deposition pressure on GSZO TFTs.

2.5.3 ZSO There has been no published literature reporting on the effects of deposition pressure on ZSO TFTs.

2.6 Active Layer Thickness

2.6.1 IGZO Chiang et al. [34] investigated how various parameters such as annealing conditions and thickness as well as oxygen partial pressure affect IGZO TFT characteristics. It was discovered that for post deposition annealing temperatures equal to and below 400 °C, experimental variables have the greatest influence on TFT performance. Above 400 °C, annealing treatment dominates TFT performance. Mobility increased and V_{ON} decreased as oxygen partial pressure decreased and RF sputter power decreased. Also, for channel thicknesses thinner than 50 nm, mobility does not vary much as it remained low and V_{ON} increased. Also, it was found that as V_{ON} approaches 0 V, device stability under constant bias stress improved.

Ding et al. [35] reported on the influence of IGZO channel layer thickness on the performance of TFTs by varying the channel layer thickness from 25 nm to 120 nm. The morphology of the IGZO films found the R_{rms} to increase with increasing thickness (0.6 nm to 0.77 nm) however the IGZO surface was found to be relatively smooth and uniform. TFT performance showed an increase in I_D with increasing channel thickness up to 58 nm and then was found to decrease. Absence of current crowding in the output characteristics indicated good ohmic contacts between the channel and S/D metals. The V_{TH} was found to decrease with increasing channel thickness up to 58 nm. This increase can be explained by the enhancement of

free carriers with channel layer thickness until semi-insulating characteristics of the IGZO layer deteriorated the V_{TH}. Relatively low carrier mobility was obtained for thinner IGZO films in comparison to the thicker films. This can be explained by the carrier transport layer being further from the surface of the thicker film thus the influence of surface roughness on the carrier mobility being weaker for thicker films compared to thinner films.

2.6.2 GSZO There has been no published literature reporting on the effects of channel thickness on GSZO TFTs.

2.6.3 ZSO There has been no published literature reporting on the effects of channel thickness on ZSO TFTs.

2.7 Flexible Substrate TFTs

2.7.1 IGZO Lim et al. [36] produced enhancement mode bottom gate a-IGZO TFTs on polyethylene terephthalate (PET). The substrate was first coated with In_2O_3 and the gate dielectric was SiO_2. High saturation mobility was observed (>22 $cm^2 V^{-1}s^{-1}$) and high on-off ratio $>10^5$. After an aging time of 500 hours, the a-IGZO TFT's mobility remained constant while the threshold voltage shifted by 150 mV.

Lee et al. [37] investigated the electrical properties of a-IGZO TFTs with transparent a-IZO electrodes on a flexible thin glass substrate. A 70 μm-thick ultra-thin glass (D-263 borosilicate) substrate purchased from Schott was used as the glass flexible substrate and TFTs were also fabricated on polymer substrate. Two types of TFTs were fabricated, one having symmetric gate overlap length and the other an asymmetric gate overlap length. Superior IGZO TFTs were obtained on the thin glass substrate compared to those on the polymer substrates in particular the 9.1 $cm^2/V{\cdot}s$ compared to the 3.1 $cm^2/V{\cdot}s$ on the polymer substrate. Bend tests were performed using semicircular shaped curvature molds which were set to 50 mm and 40 mm

critical radiuses. From the bending tests V_{TH} was negatively shifted as increase of the bending strain for the symmetric gate overlap sample, while the TFTs showed relatively stable operation against mechanical strain for the asymmetric gate overlap sample.

2.7.2 GSZO There has been no published literature reporting on the effects of channel thickness on GSZO TFTs.

2.7.3 ZSO Jackson et al. [38] reported on flexible ZSO transistors fabricated by sputter deposition on polyimide substrates with a blanket aluminum gate electrode. Al was sputter deposited over polyimide sheets followed by deposition of 375 nm of silicon oxynitride (SiON) by PECVD at 300 °C. ZSO (50 nm) was also sputter deposited as the substrate was held near room temperature. Post deposition annealing was performed in air at 250 °C for 10 min. Excellent performance was obtained with mobilities as high as ~14 $cm^2/V \cdot s$ while providing low contact resistance with indium tin oxide (ITO) contacts.

2.8 Applications

2.8.1 IGZO Ito et al. [39] investigated the application of IGZO a-TFTs with an electrophoretic front plane. An E Ink display was successfully driven by a 4" Quarter Video Graphics Array (QVGA). QVGA's are commonly used as a computer display. The source and drain contacts were formed via screen printing which lowers fabrication cost. A high on off ratio of more than seven orders of magnitude was achieved and a field effect mobility of 2.8 $cm^2/V \cdot s$ was observed.

Arai et al. [7] provide support for active matrix organic light emitting diode (AMOLED) backplane applications. They assert that a channel mobility ~16 $cm^2/V \cdot s$ is adequate for realizing AMOLED displays with UHD resolution (3840x2160=8.3 megapixels) at a frame rate of 480 Hz or with 8k UHD resolution (7680x4320=33.2 megapixels) at a frame rate of 240 Hz. Moreover

they also developed indium tin zinc oxide (ISZO) TFTs with even higher mobility of 30.9 $cm^2/V \cdot s$. Industrial reports of IGZO TFT technology improvements applied to commercial AMLCD and AMOLED displays are becoming a regular occurrence at Society of Information Display (SID) and other international display conferences.

2.9 Conclusion

In conclusion this chapter examined reported literature on different AOS TFTs such as IGZO, GSZO and ZSO. Causes for improved electrical and optical stability were examined as well as the effects of deposition and annealing temperatures, deposition pressures and channel thicknesses. The reports of AOS devices fabricated on plastic and its applications were reviewed.

CHAPTER 3

Experimental Details

3.1 Introduction

In this chapter a brief description of the GSZO deposition process as well as the fabrication of the GSZO TFTs is given. The RF sputtering system configuration is described and the deposition conditions used for film characterization as well as the equipment used to anneal the film and deposition of the contact metal. The TFT fabrication procedure is discussed, which includes from the selection of the n^+ Si wafer to the lift-off of the metal used for contacts.

3.2 GSZO TFT Configuration

The bottom gate TFT investigated in this work, consists of a 130 nm thick n^+ Si with 0.01-0.05 Ω·cm resistivity. 130 nm of SiO_2 is then oxidized onto the Si wafer and GSZO was then deposited following a photolithography process to mask the TFTs except for areas designated to the metal contacts. 100 nm of Al or Au/Ti is then deposited through electron-beam evaporation. These two contacts are called source and drain and the n^+ Si wafer is called the gate. The SiO_2 constitutes the gate oxide and the GSZO is referred to as either the channel or active layer. A 2-D schematic of the bottom-gate GSZO TFT used for device characterization is shown in **Error! Reference source not found.**.

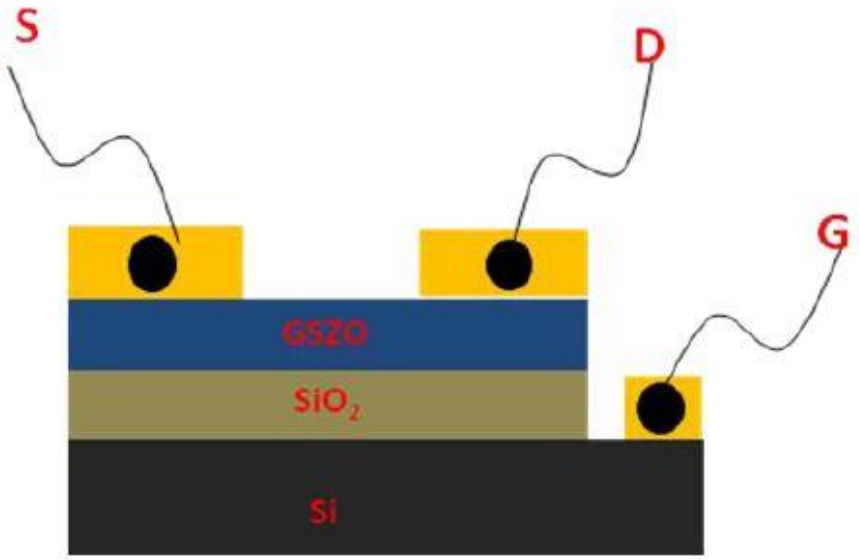

Figure 4 2-D schematic of GSZO TFT

3.3 SiO_2 Oxidation

Prior to active layer deposition the Si wafer was oxidized which serves as the gate oxide between the n^+ Si wafer and the active layer. This oxidation process is performed within a furnace by heating the silicon wafers to a high temperature of 1100 °C in the presence of pure oxygen. Within an hour, 130 nm of SiO_2 is formed through a chemical reaction occurring at the silicon surface. The silicon surface is consumed as the oxide grows; resulting in the final oxide layer being approximately 54% above the original surface of the silicon and 46% below the original surface as shown in Figure 5. As described above, a low resistivity (0.01-0.05 Ω·cm) n^+ Si wafer was chosen to serve as the gate electrode to effectively induce an electric field through the gate oxide, into the channel layer and to reduce the contact resistance of the fabricated device.

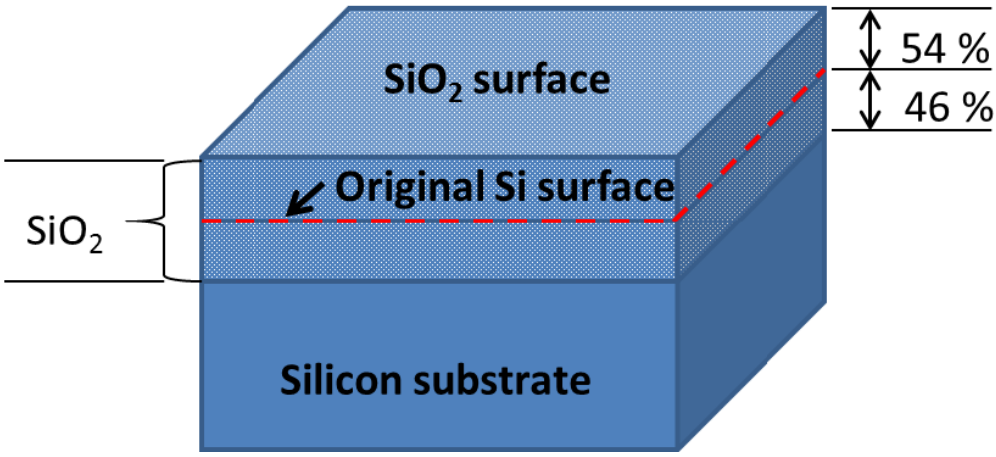

Figure 5 Oxidation of SiO_2 onto surface of Si

3.4 RF Magnetron Sputtering

The sputtering system used to deposit films in our investigative process was the Edwards ESM Sputtering Tool. A cylindrical and stainless steel chamber of 12 x 13.5" in diameter was used to confine all gases during the above stated procedures. The opening of the chamber is a stainless steel lid with an interlock preventing the use of any power generator while the lid is opened. Two glass windows are located on the front and back of the chamber to allow visibility of the entire deposition process. Figure 6 shows an outside view of the chamber with ionized plasma inside, and an inside view of the chamber from above.

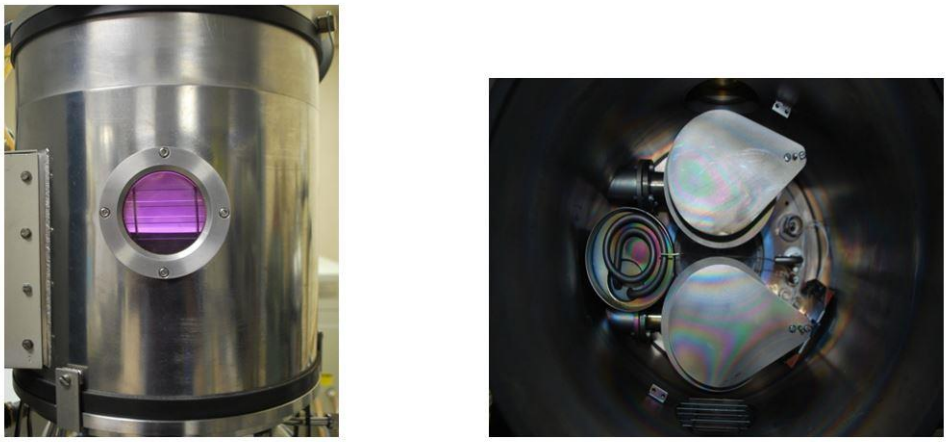

Figure 6 Outside and inside view of chamber of the Edwards ESM Sputter Tool

The substrate holders are located on the lid of the chamber. These holders are visible when the lid is open and are located within the chamber when the lid is sealed corresponding to a sputter up configuration. There are two stainless steel substrate holders and both are connected to the anode of the system. A motor is located above the lid of the system which permits the substrate holders to rotate when desired. Figure 7 shows the substrate holders located within the chamber.

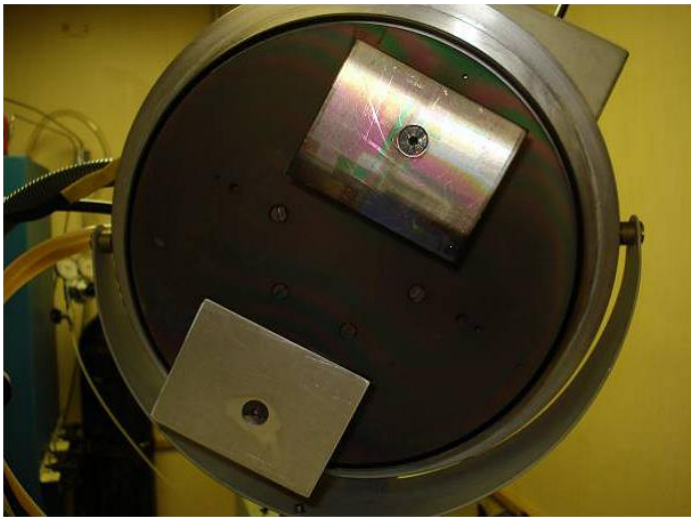

Figure 7 Substrate holders of the Edwards ESM Sputtering Tool

The substrate holders are the anodes of the sputtering system, and the targets form the cathodes of the system. There are 2 target holders located within the chamber, each having its own shutter. The target holders support 4" diameter targets with ¼" thicknesses including a copper plate located on the targets back side. During depositions, the target of choice for the deposition is isolated electrically from the chamber and the unused target is shorted. This allows the stable potential difference needed across the anodes and cathode. The composition of the SGZO target used for experimentation is ZnO (88%) +Ga_2O_3 (5%) +SnO_2 (7%) 99.9% pure,

4.00” in diameter and 0.125” thick with a density of 5.44 g/cc. Figure 8 shows the GSZO target and the target holder located within the chamber.

Depositions were conducted at either room temperature or an elevated temperature. During elevated temperature depositions, a custom made radiant heater was used to heat the inside of the chamber. The radiant heater was controlled by a Watlow temperature controller and heat was measured using a thermocouple. Figure 9 shows the radiant heater used for heated depositions.

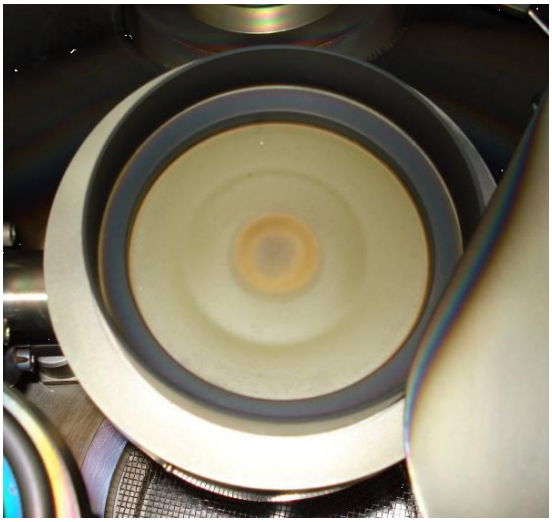

Figure 8 A target holder within the chamber of the Edwards ESM sputtering tool

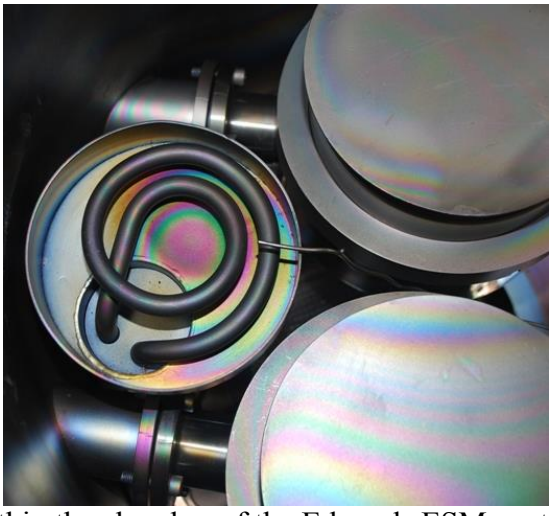

Figure 9 Radiant heater within the chamber of the Edwards ESM sputtering tool

Two pumps were used to achieve the desired vacuums for our investigations. The Edwards (E2M28) high vacuum mechanical pump was used to rough the chamber down to a vacuum of 10^{-2} Torr. After this vacuum was met within the chamber, a CTI Cryo-Torr 8 trapping pump was used to achieve a maximum vacuum of $2x10^{-7}$ Torr within the chamber. During the deposition and etching processes, the pressure is regulated using the MKS type 252 exhaust valve controller and ACX display. As different gases are introduced into the chamber, flow is regulated using MKS mass flow controllers which digitally displayed the volumetric flow in standard cubic centimeters per minute. Figure 10 shows the high vacuum mechanical pump and the CTI-Cryogenics pump used to reach ultra-high vacuum within the system.

Etching processes were carried out using the Edwards Plasma Products Inc. model RF 55, 500 W RF generator. An automatic impedance matching network was coupled with the RF generator to ensure maximum power was transferred to the system. Deposition processes were carried out using the Edwards Plasma Products Inc. model RF-10, 1000 W RF generator which too was coupled with an automatic impedance matching network.

Figure 10 The Edwards (E2M28) high vacuum mechanical pump and the CTI Cryo-Torr 8 trapping pump.

3.5 Post-Deposition Annealing Furnace

An in-house built annealing furnace was used to anneal samples in air and is shown in Figure 11. The system consists of an Au coated, partially transparent quartz tube. It is a single zone furnace equipped with K-type thermocouples used to monitor the temperature within the quartz tube. A quartz tube with a flat boat is used to load and unload samples from the annealing furnace. All devices were annealed in air at 140 °C for future TFT fabrication on plastic.

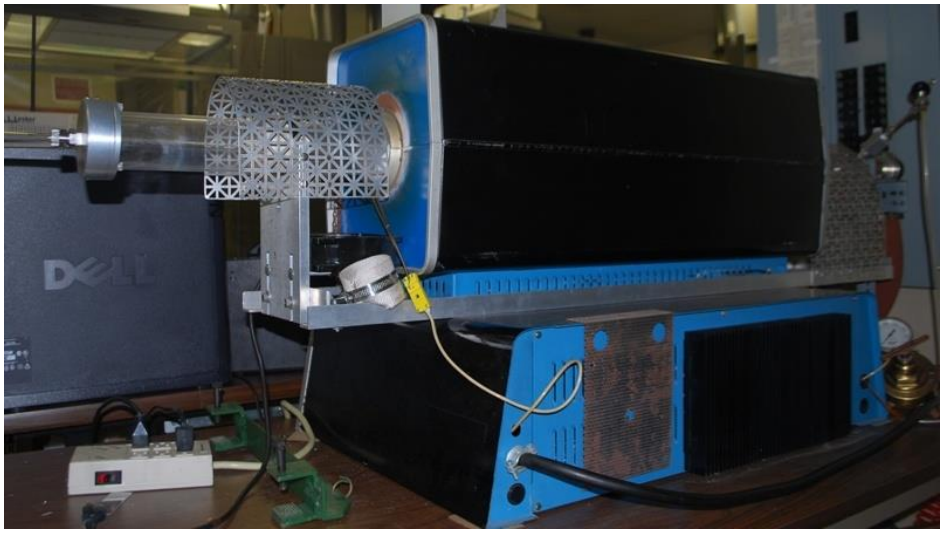

Figure 11 Post deposition annealing furnace

3.6 Photolithography of TFTs

After the annealing the samples are prepared for TFT fabrication which includes photolithography, plasma cleaning, contact metal deposition and gate formation. After being cleansed in acetone and propanol separately in an ultrasonic bath, a coat of hexamethyldisilazene (HMDS) was spun onto the GSZO to promote the adhesion of the positive photoresist. Afterwards the sample is hard baked for 1 minute at 90 °C and exposed to ultraviolet (UV) light to form the channel of the TFTs first. The sample is again hard baked at 90 °C for 1 minute and then placed in positive developer to remove all of the positive photoresist except for the channels. The sample is then placed into a solution of deionized water (DI H_2O) and

hydrochloric acid (HCL) 500:1. This removes the GSZO that is not under the leftover positive photoresist thus exposing the SiO_2. The sample is then placed into acetone to remove the leftover photoresist and then propanol for a final cleaning.

HMDS is then spun onto the sample again, this time to promote the adhesion of the negative photoresist. The sample thereafter hard baked for 1 minute and then negative photoresist is spun and hard baked. The sample is again exposed to UV light to assist in the formation of the source/drain contacts and hard baked for 90 seconds. The sample is then placed into negative developer for 20 seconds to remove the un-exposed parts of the photoresist which forms the source/drain contacts. Subsequently the sample is treated in pure O_2 plasma to assist in the removal of remaining organics and solvents to assure proper adhesion of the metal for the source and drain. The plasma cleaning system used is the South Bay Technology PE-150 plasma etcher. The mask layout for the TFTs is shown in **Error! Reference source not found.** and the photolithography process is illustrated in **Error! Reference source not found.**.

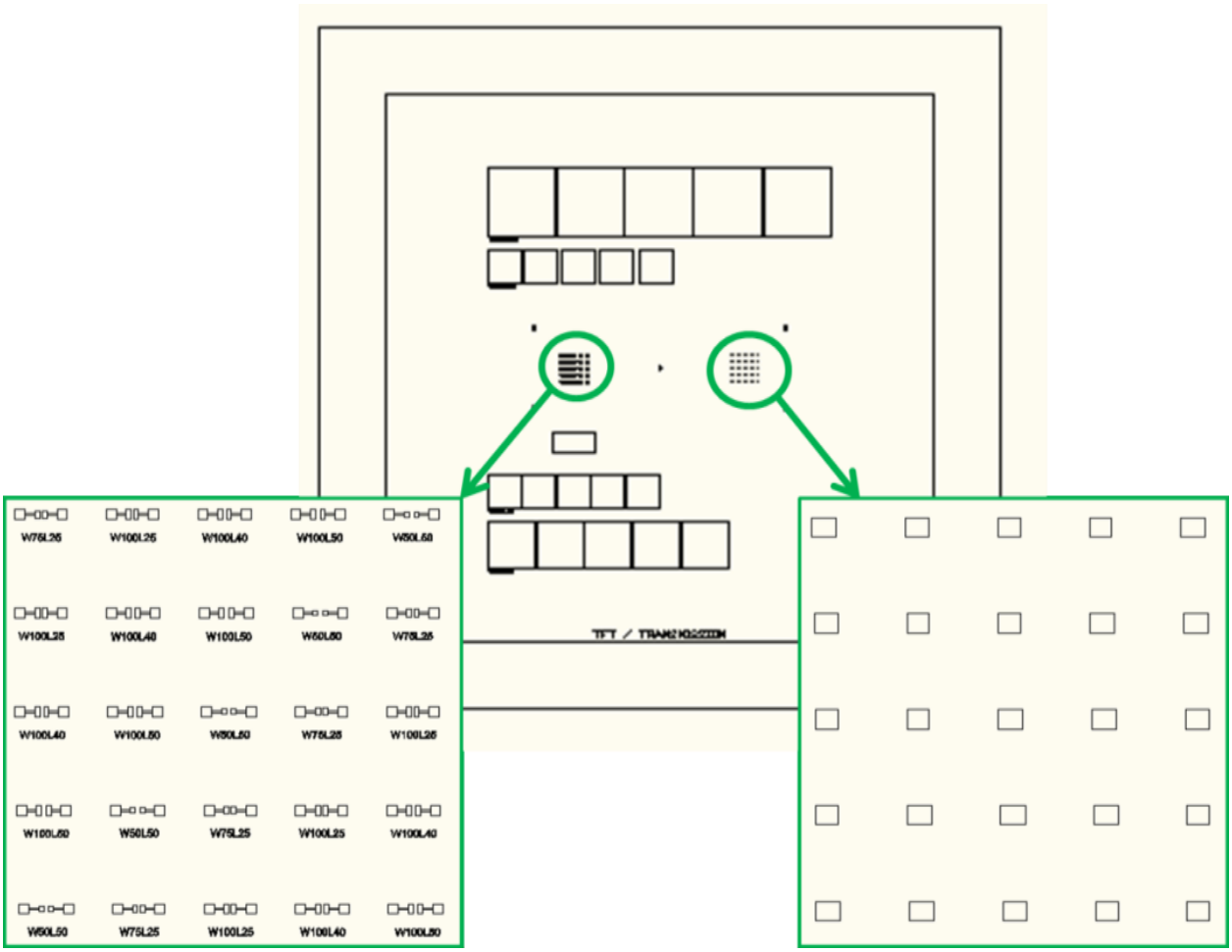

Figure 12 TFT Mask Layout

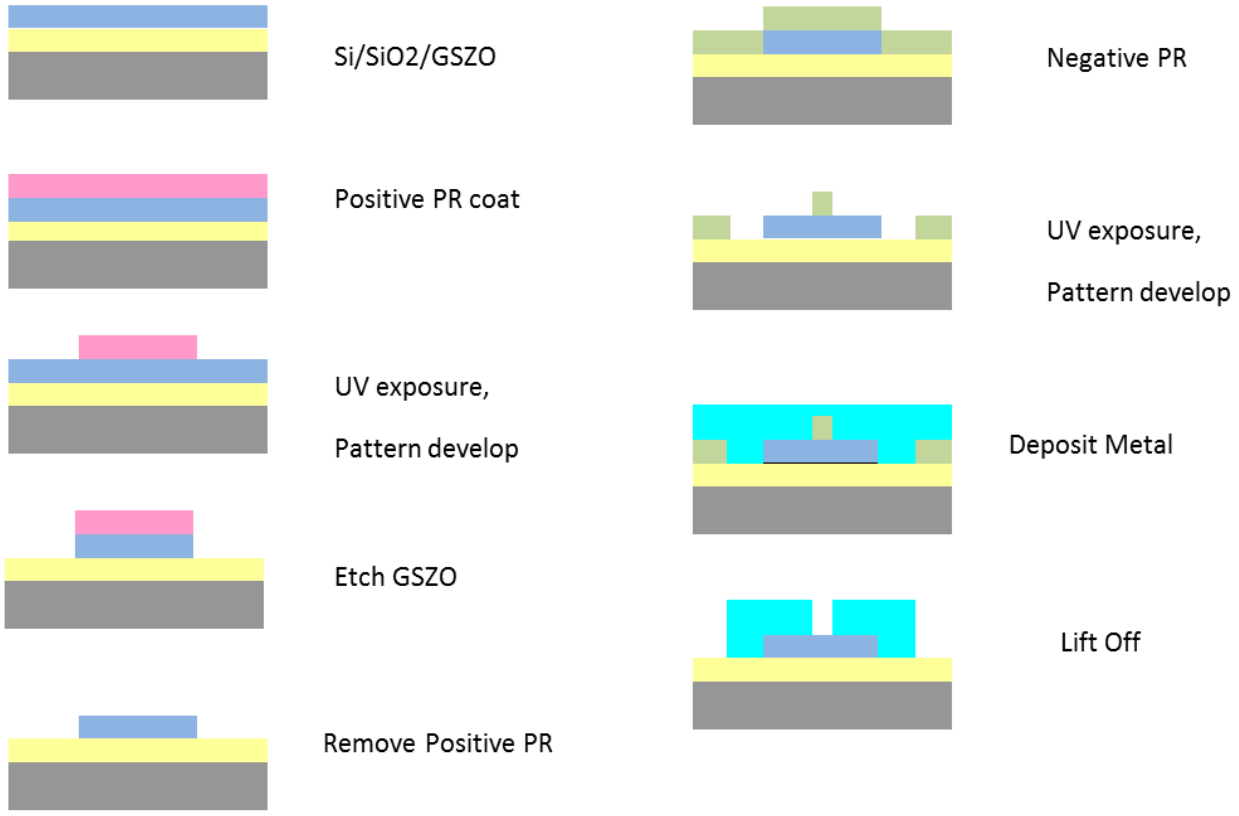

Figure 13 Photolithography process for fabricated bottom-gate GSZO TFTs.

3.7 Electron-Beam Evaporation (E-Beam)

The Kurt Lesker PVD75 E-Beam Evaporator (Figure 14) system is used to deposit the metals for the source/drain contacts. In this work, Au/Ti and Al were 2 separate metals investigated for contacts. The thickness of the Au/Ti was 100/20 nm and the Al was 100 nm. The metal was then lifted with acetone at all places except for the source and drains and lastly cleansed with propanol. The Si substrate was used as the gate which was formed by placing hydrofluoric acid (HF) onto the SiO_2 to expose the underlying Si.

Figure 14 Kurt Lesker PVD 75 e-beam evaporator [40]

3.8 Conclusion

RF sputtering technique was used to deposit thin films of GSZO for AOS TFT fabrication due to its ability to deposit onto a large surface area at low temperatures. Deposition parameters such as deposition temperature, deposition pressure, channel thickness and annealing duration were investigated to determine the effect of these parameters on the performance of TFTs fabricated which will be the focus of the discussion of the following chapters.

CHAPTER 4

TFT and Material Characterization

4.1 Introduction

This chapter will provide a description of the characterization techniques used to analyze the performance of the GSZO TFTs and various properties of the GSZO films utilized in this work. Electrical properties of the GSZO TFTs such as I-V transfer and output curves, multi-frequency C-V curves and electrical and optical stability were examined. Aside from GSZO films being deposited for TFT fabrication, thin films were also deposited onto Si and 7059 glass to further investigate the electrical, optical and structural properties of the GSZO film. Various characterization techniques such as XRR, XPS, RBS, AFM, ellipsometry, absorption and stability were used and are described in this chapter. All GSZO films were deposited at 45 W in Ar/O2 plasma of 10:1. It is to be noted that XPS and RBS material characterizations were carried out by expert personnel from Evans Analytical Group Inc.

4.2 Current-Voltage Measurements

The Keithley 4200- Semiconductor Characterization System (Figure 15) and SemiProbe LA-150 probe station were used to graph the output curves, drain-source current (I_{DS}) vs. drain-source voltage (V_{DS}) and transfer curves, namely I_{DS} vs. gate-source voltage (V_{GS}) using a hold and delay time of 0.5 s and 0.2 s. An example of transfer characteristics exemplifying how to find V_T, $I_{ON/OFF}$ and on-voltage (V_{ON}) is shown in Figure 16. Electrical characteristics such as maximum drain current (I_D or I_{ON}), minimum drain current (I_{OFF}), ratio of I_{ON} and I_{OFF} ($I_{ON/OFF}$), V_{ON} (voltage at which $I_D \sim 5x10^{-12}$ A), sub-threshold swing (SS) which is a measure of the required voltage needed to increase I_D an order of magnitude and field-effect mobility (μ_{FE}) were investigated. Equations 1 and 2 have been used to find μ_{FE} and SS. In Equation 1, g_m-

transconductance, W/L-width to length ratio of active layer, C_i-capacitance per unit area of SiO_2, $V_{D(0.5\ V)}$- drain voltage at 0.5 V. In Equation 2, ΔV_D-change in drain voltage, $\Delta\log(I_D)$-change in I_D per decade. V_{ON} is considered the voltage at which I_{DS}~$5x10^{-12}$ A unless otherwise specified.

$$\mu_{FE} = \frac{g_m}{\frac{W}{L}C_i V_{D(0.5\ V)}} \qquad \text{Equation 1}$$

$$SS = \frac{\Delta V_D}{\Delta log I_D} \qquad \text{Equation 2}$$

For the output curves, V_{DS} was swept from 0-20 V while I_{DS} was collected and V_{GS} also increased from 0-20 V for each sweep of V_{DS}. For the transfer curves, V_{GS} was swept from -20 to 20 V and I_{DS} was collected while V_{DS} remained at a constant bias of either 0.5 V or 20 V. The previous curves were collected while the TFT device was held in the dark unless specified otherwise.

Figure 15 Keithley 4200 semiconductor characterization system used for I-V characterizations.

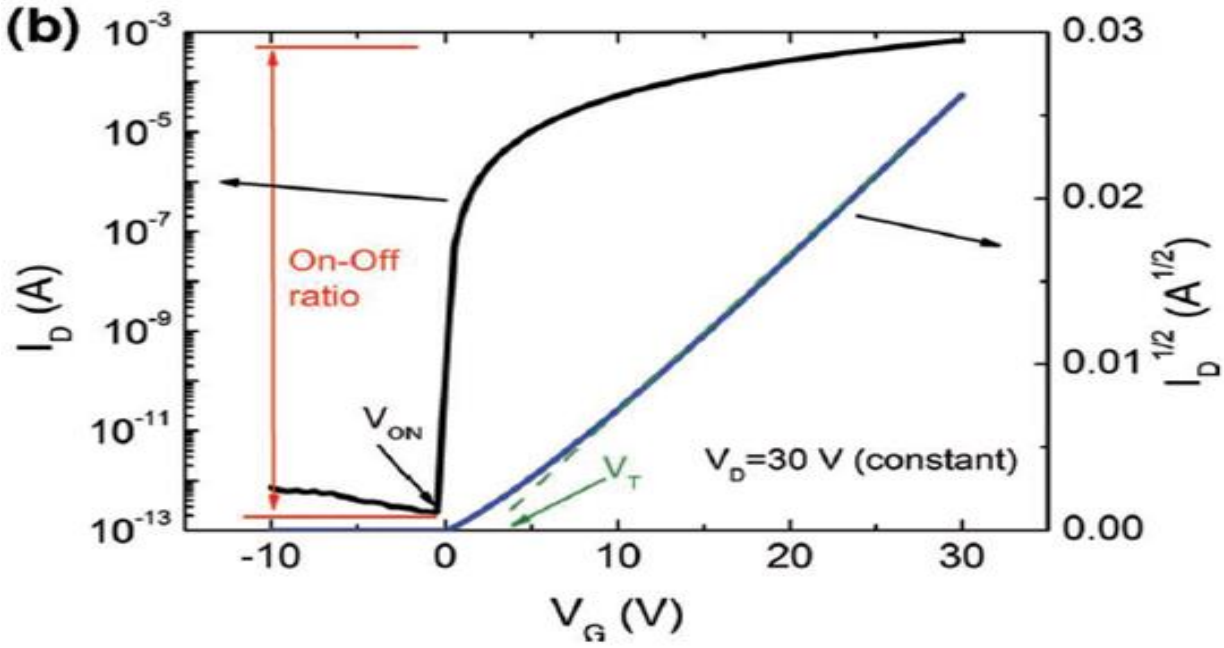

Figure 16 Example of transfer characteristics explaining how to find different electrical parameters.

4.2.1 Electrical Stress Applying an electrical bias at V_{GS} for a given time is considered applying electrical stress to the TFT. GSZO TFT transfer curves were captured prior to applying an electrical bias followed by a re-test of device transfer curves after the bias for a given duration. Positive bias stress (PBS) is the application of a positive bias at the gate while a negative bias stress (NBS) is the application of a negative bias to the gate and the source and drain are grounded. Both PBS and NBS have been applied to TFTs to analyze the electrical stability of the devices.

4.2.2 Optical Stress To understand the optical stability of the films as well as determining the energy levels of charges trapped in V_O's and the trapping mechanisms prevalent within the channel or the channel/interface under different deposition conditions, photo-excited

TFT transfer characteristics were captured under illuminations of different wavelengths in the presence and absence of external electrical bias. The setup of the Micro HR Horiba Scientific monochromator (Figure 17) which was used to selectively choose wavelengths to optically stress the devices before and during I-V tests. Photons of wavelengths 410 nm (3.02 eV), 550 nm (2.25 eV) and 650 nm (1.90 eV) were focused on the GSZO channel of the TFT for 10, 30, 60, 90 and 120 minutes and subsequently electrically tested. Transfer measurements were taken under photo-excitation stress after a given duration to examine the devices photo-stability. To ensure the effects of photo-excitation were observed, V_D was maintained at a low voltage of 0.1 V and 0.5 V.

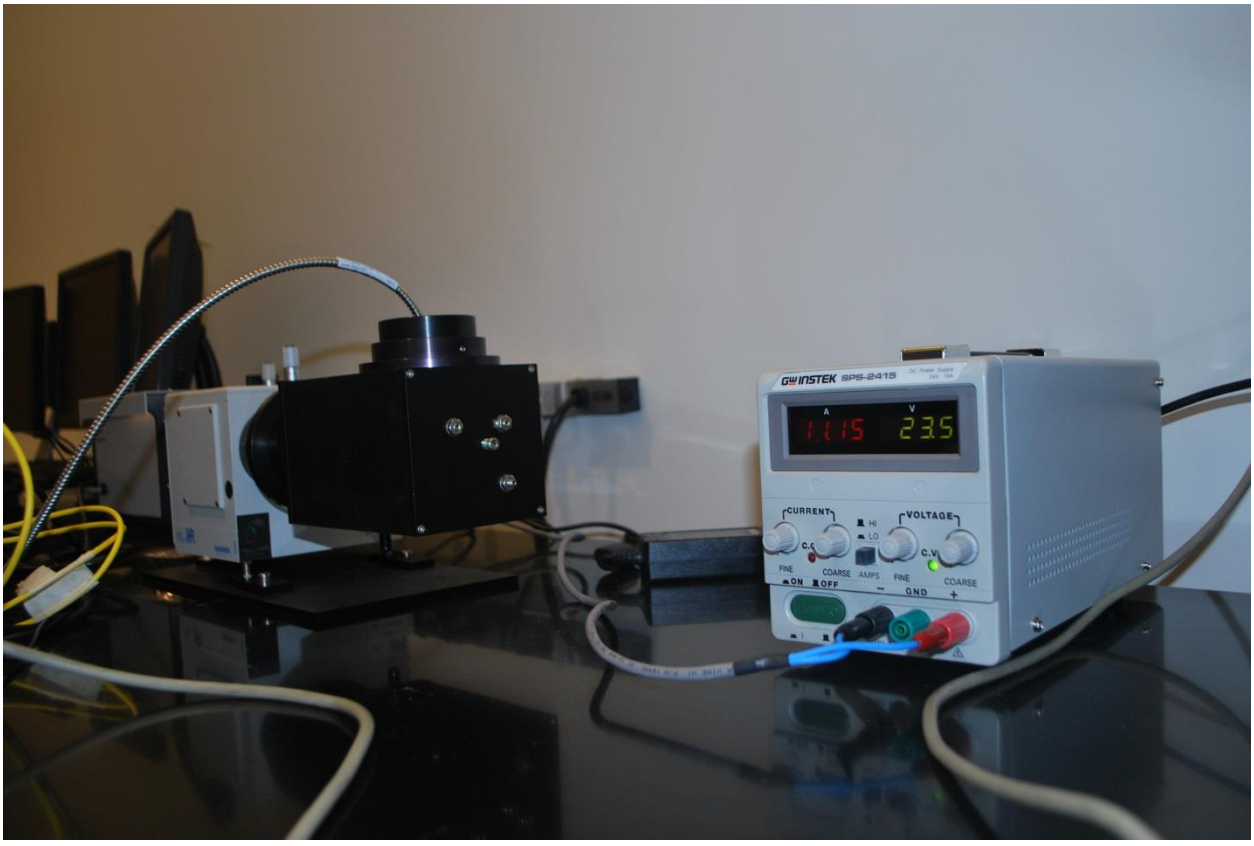

Figure 17 Micro HR monochromator used for optical stress characterization

4.3 Capacitance-Voltage Measurements

To investigate the C-V performance of the GSZO TFTs, the HP 4284 LCR meter was used. *Figure 18* shows the device test setup which consists of the device under testing (DUT) on a stainless steel platform with high-sensitivity probes placed on the contacts of the DUT connected to triaxial cables which are connected to the HP 4284 LCR device. In-house programmed software triggers the controls of the LCR meter which supplies the DC voltage and AC current to the DUT. The program then records and provides a graphical display of the measurement at the end of each experiment. The values used for C-V experimentation are shown in Table 2. The computer program also provides an interface that allows the user to input the measurement parameters such as frequency, DC and AC voltage values. A 2-D schematic of the DUT and connections are shown in Figure 19.

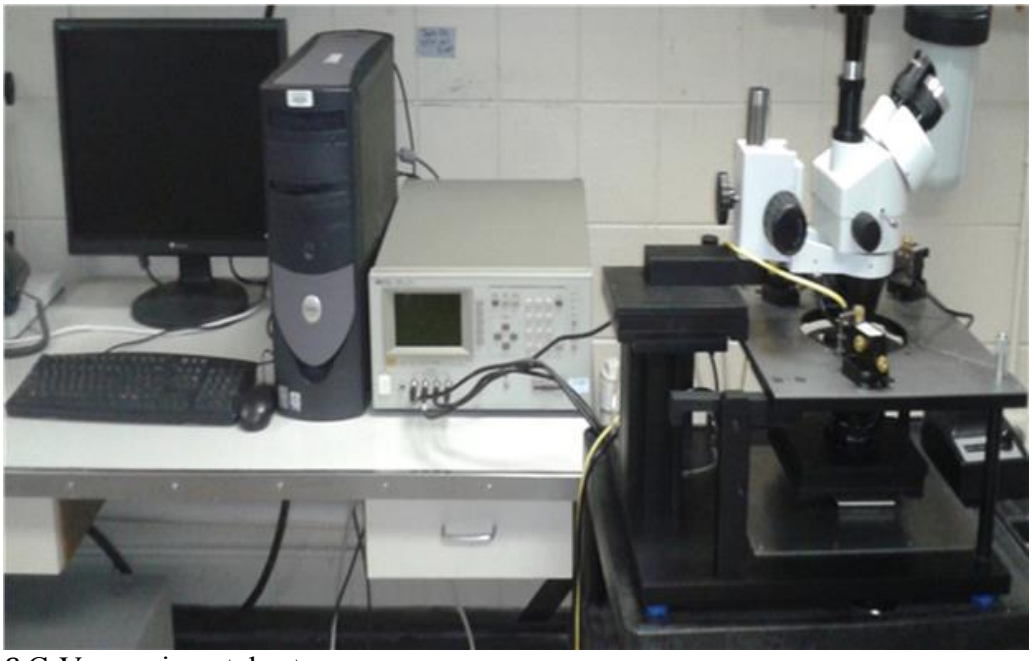

Figure 18 C-V experimental setup

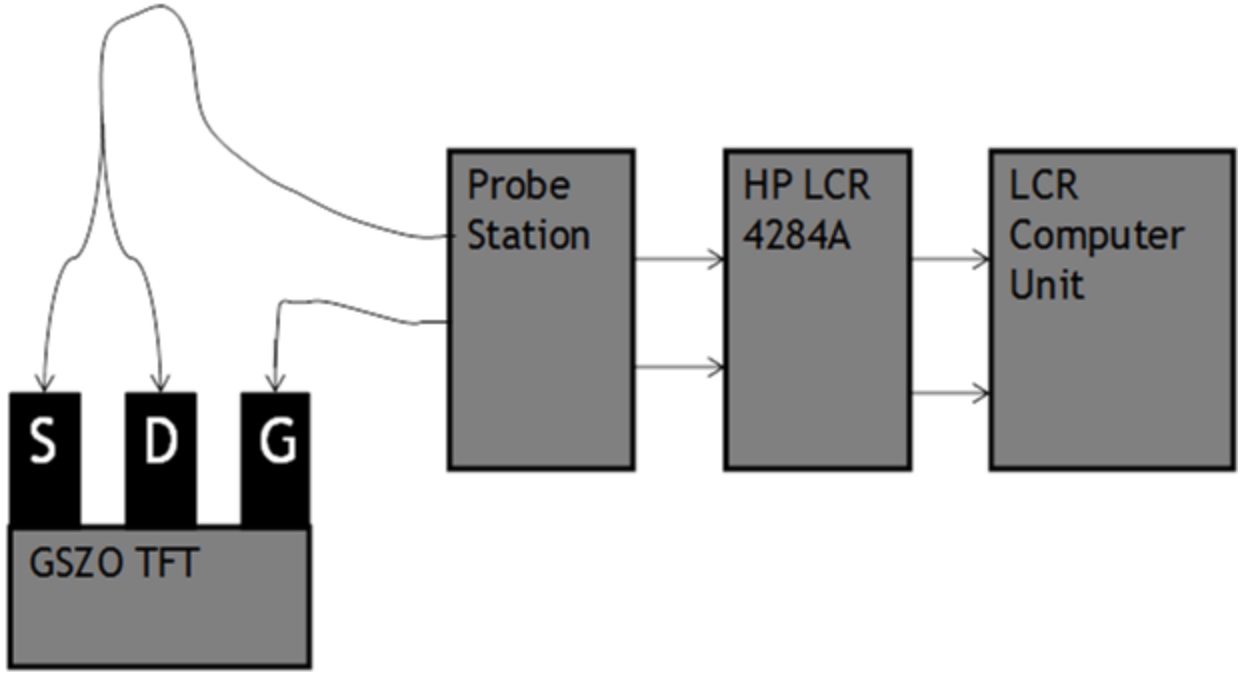

Figure 19 2-D schematic of DUT for C-V experiments

Table 2

C-V experimental values

AC Current	40 mA
Gate Voltage	-20 to 20 V
Drain/Source Voltage	Ground
Frequencies	250 to 1M Hz

4.4 Ellipsometry

To determine the thickness of the films sputtered, ellipsometry measurements were conducted on thin films sputtered on silicon substrates. Ellipsometry is an optical technique used to measure the complex refractive index and thickness of thin films. Light waves are reflected from the thin film to a sensor that analyzes the reflected phase and polarization light wave

characteristics. Ellipsometry is contactless and does not destruct the film being analyzed. A requirement of the film being investigated is that it is homogenous and isotropic. Films with thicknesses ranging from a single atomic layer to a few angstroms to several micrometers can be analyzed with great accuracy.

The Rudolph Research Auto EL II model ellipsometer used to conduct ellipsometry experiments is shown in Figure 20. A He/Ne laser operating at a wavelength of 632.8 nm was used to penetrate the GSZO films and reflected to a sensor for analysis. The system displays angles Ψ and θ, which describe changes in the amplitude and phase of the reflected light wave. In conjunction with the system, software titled "Rudolph Research Double Absorbing Films Calculations" is used for the conversion of the Ψ and θ variables to the thickness of the thin films.

Figure 20 The Rudolph Research Auto EL II Ellipsometer used for film thickness analysis

4.5 Atomic Force Microscopy (AFM)

The surface morphology was analyzed using an Agilent Technologies 5600 LS Atomic Force Microscope (Figure 21). The Agilent 5600 LS is equipped with a 200 mm x 200 mm fully addressable and programmable stage for ease of use including mounting / unmounting the samples. The system was used in automated tip mode to minimize damage to the sample surface during the scan. Image scan areas of 20 μm^2 and 5 μm^2 were done to observe the surface roughness and morphology. After the data acquisition AFM analysis was done using the free open source software Gwyddion.

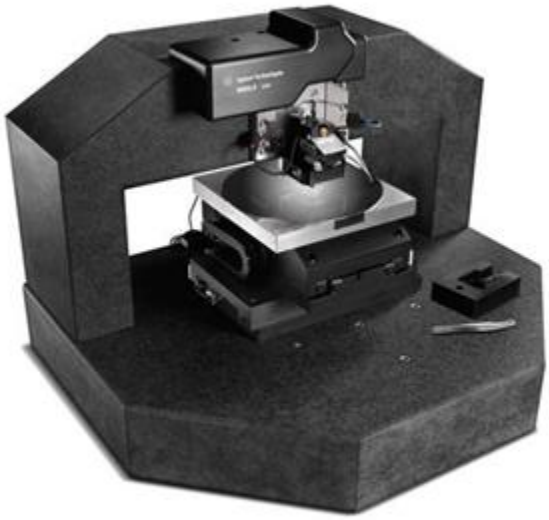

Figure 21 Agilent Technologies 5600 LS Atomic Force Microscope used for AFM characterizations.

4.6 X-ray Reflectivity (XRR)

X-ray reflectivity was used as to determine the thicknesses, film density, and gate oxide/GSZO interface roughness. This was done by overlapping the computer simulated data

using the above film parameters as fitting parameters. The Bruker AXS D9 Discover X-Ray diffractometer system was used for XRR testing and is shown in Figure 22.

Figure 22 The Bruker AXS D9 Discover X-Ray diffractometer system used for XRR characterizations.

4.7 Atomic Composition (RBS & XPS)

4.7.1 Rutherford Backscattering (RBS) Evans Analytical Group Inc. conducted elemental composition analysis on selective GSZO films. One method was RBS in which an RBS spectrum was acquired at a backscattering angle of 160 ° and at an appropriate grazing angle (with the sample oriented perpendicular to the incident ion beam). The film is rotated or tilted with a small angle to display a random geometry to the incident beam. This is done to avoid channeling in both the film and the substrate. The use of two detector angles can significantly improve the measurement accuracy for composition when thin surface layers need to be analyzed. Figure 23 shows the scattering geometry used in this RBS experiment and the analytical parameters are shown in Table 3.

Spectra are fit by applying a theoretical layer model and iteratively adjusting elemental concentrations and thickness until good agreement is found between the theoretical and the experimental spectra. The determination of layer thickness from RBS data requires making assumptions about the film densities. If the thickness of the films is known, the real density can be calculated. Conversely, if the density is known RBS can provide accurate thicknesses. The equation governing the conversion from the RBS densities (D_{RBS}), RBS thicknesses (T_{RBS}) and real thicknesses (T_{real}) to the real densities (D_{real}) is given below in Equation 3.

$$D_{real} = (D_{RBS} \times T_{RBS})/T_{real} \qquad \text{Equation 3}$$

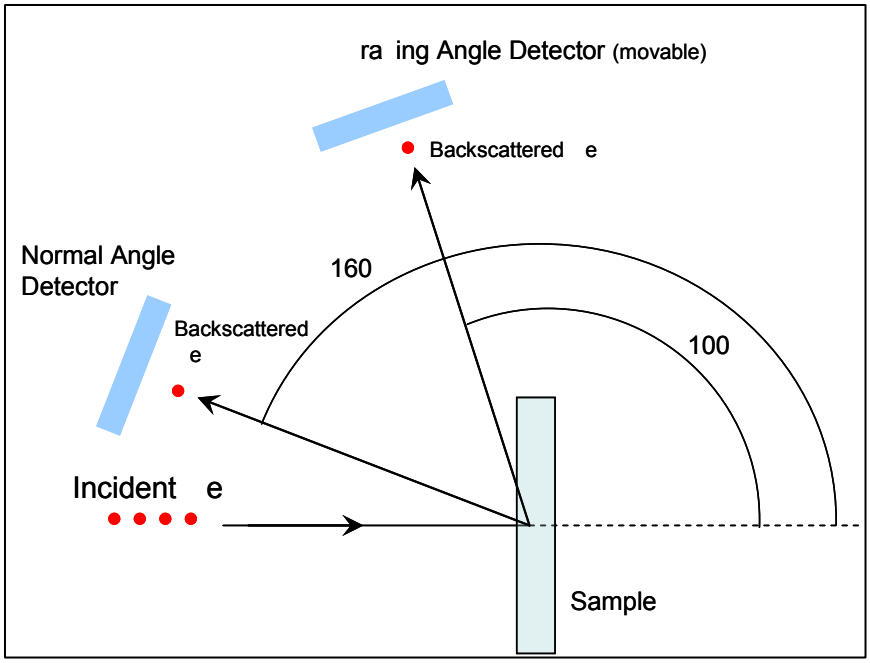

Figure 23 Scattering geometry in a typical RBS experiment

Table 3

Analytical Parameters: RBS

He^{++} Ion Beam Energy	2.275MeV
Normal Detector Angle	160°
Grazing Detector Angle	~100°
Analysis Mode	*CC RR*

4.7.2 X-Ray Spectroscopy (XPS) The goal of this analysis was to determine the surface composition of the as-received GSZO films and after the sputtering of 5 nm. XPS data is quantified using relative sensitivity factors and a model that assumes a homogeneous layer. The analysis volume is the product of the analysis area (spot size or aperture size) and the depth of information. Photoelectrons are generated within the x-ray penetration depth (typically many

microns), but only the photoelectrons within the top three photoelectron escape depths are detected. Escape depths are on the order of 15-35 Å, which leads to an analysis depth of ~50-100 Å. Typically, 95% of the signal originates from within this depth. The analytical parameters used for XPS characterization are shown in Table 4.

Table 4

Analytical Parameters: XPS

Instrument	PHI 5701LSci
X-Ray Source	Monochromated AlKα 1486.6 eV
Acceptance Angle	±7°
Take-Off Angle	50 °
Analysis Area	2mm x 0.8 mm
Charge Correction	C1s 284.8 eV
Ion Gun Conditions	Ar^+, 3keV, 4 x 4 mm raster
Sputter Rate	29 Å/min (SiO_2 Equivalent)

4.8 Optical Transmission

Optical transmission measurements are commonly used towards the determination of absorption coefficients. Shallow level impurities also respond to optical measurements providing more specific information on a sample's quality.

Transmission measurements are taken as a light source is incident upon the sample and the transmitted light is measured as a function of wavelength. The sample is characterized by

reflectivity *R* and an absorption coefficient α. Transmission and reflection measurements were taken from Varian Cary 6000i UV-Vis-NIR spectrophotometer system as shown in Figure Figure *24*.

Figure 24 Varian Cary 6000i UV-Vis-NIR Spectropohotometer [41]

The Varian Cary 6000i spectrometer is a double beam, double monochromator ratio recording system. It is equipped with a tungsten-halogen and a deuterium lamp source. A scan range from 175 to 3300 nm is capable within an accuracy of 0.08 nm in the uv-visible region and 0.3 nm in the near infrared (NIR) region. A mercury lamp module was used for wavelength accuracy validation and the scan range for this experiment was from 320-2400 nm. The

transmission spectra of the film in this study were determined by subtracting the spectra of the scanned sample with a deposited film from a reference sample without film.

4.9 TFTs on Plastic Substrate

Personnel at Research Triangle Institute International (RTI Int'l) assisted in the fabrication of bottom gate GSZO TFTs on PEN substrates. PEN was placed on a Si substrate using adhesive to prevent stress damage to the devices. First molybdenum (Mo) was deposited onto the PEN and the gate was formed through photolithography followed by the deposition of either SiO_2 or Si_3N_4. Some devices contain a 5 mm su-8 planarization layer to reduce surface roughness before depositing Mo and the gate insulator. The GSZO depositions and photolithography processes were carried out in our laboratory while RTI Int'l performed reactive ion etching (RIE) for channel formation. E-beam depositions were done to form the S/D contacts using 100 nm of Al. The devices were then characterized for I-V and C-V performance. A 2-D schematic of the GSZO TFTs on PEN is shown in Figure 25.

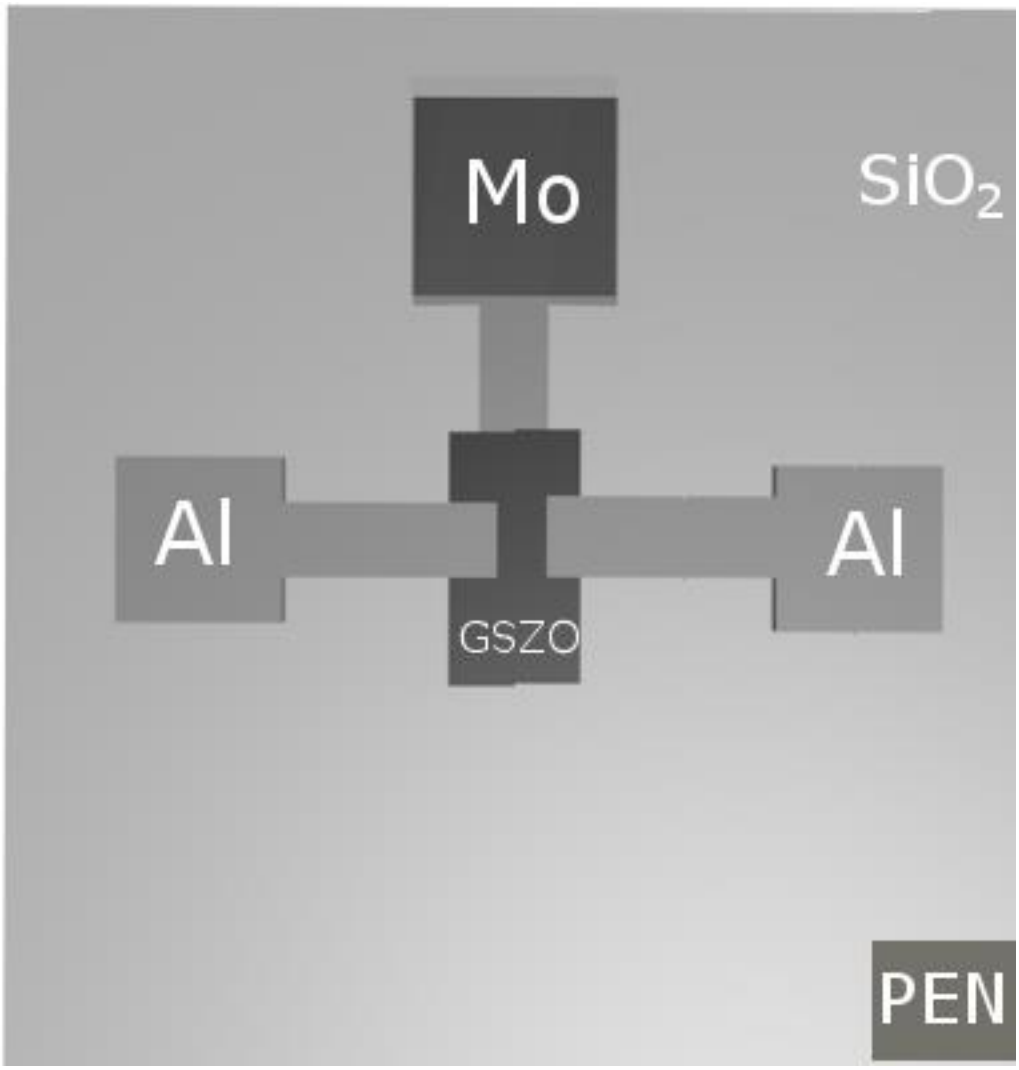

Figure 25 2-D schematic of GSZO TFT on PEN substrate

4.10 Conclusion

This chapter discussed in detail the various material characterizations used in this work. These characterization techniques were used to determine the elemental composition, surface roughness, interfacial quality, and optical absorption. A variety of characterization techniques including I-V , C-V, electrical and optical stability have been used to correlate the various properties of the TFT device and to get a deeper insight into the traps that controls the performance of the device.

CHAPTER 5

Results on Temperature Dependence and Implementation on PEN Substrate

5.1 Introduction

This chapter presents the results of various experiments and characterizations on GSZO TFTs and GSZO thin films. The bottom-gate GSZO TFTs fabricated on n^+ Si substrates were analyzed by varying procedure operations such as annealing and deposition temperatures, annealing duration, channel thicknesses and deposition pressures. GSZO films were investigated using material characterizations namely, RBS and XPS for elemental composition, XRR and AFM for surface morphology and absorption characterization for optical properties. Bottom-gate GSZO TFTs were fabricated onto PEN and its electrical characteristics were also analyzed.

5.2 Annealing

5.2.1 Annealing Temperature Reduction Previous work reported on amorphous GSZO TFTs from our group [42] was with channels which were annealed at 250 °C for 1 hour, while this work is focused on GSZO TFTs annealed at 140 °C for 1 hour. Table 5 summarizes the electrical characteristics of the TFTs with different annealing temperatures. With decreasing annealing temperature the threshold voltage slightly improved after shifting positively from -2 V to -1 V however SS degraded from 1.0 to 4 V/dec. Also I_{ON} decreased by an order of magnitude as the annealing temperature reduced, resulting in an $I_{ON/OFF}$ decrease by 1 order of magnitude.

Table 5

Electrical characteristics of TFTs annealed at different temperatures

Annealing Temperature	I_D (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/dec)
250 °C	10^{-7}	10^5	-2	1
140 °C	10^{-8}	10^4	-1	4

5.2.2 Annealing Duration To improve the performance of the GSZO TFTs without exceeding an annealing temperature of 150 °C, the annealing duration was varied. The TFTs were annealed for 1, 6 and 10 hours in air. Table 6 displays TFTs annealed at 140 °C for different annealing durations and the transfer curves are shown in (Figure 26). The maximum drain current increased from 10^{-8} to 10^{-7} A and saturated even up to 10 hours of annealing study. The $I_{ON/OFF}$ ratio correspondingly increased from 10^3 to 10^5 with no apparent change in I_{OFF} with increase in annealing duration. The V_{ON} shifted negatively with increasing annealing duration, stopping at -9.5 V after 10 hours. The μ_{FE} improved with annealing duration by almost 2 orders of magnitude as SS decreased by half.

To reduce contact resistance and improve film adhesion, the GSZO TFTs were placed on a hotplate at 140 °C for 1 minute. This procedure we refer to as post-contact annealing (PCA) and the results are shown in Table 7. I_{ON} increased and order of magnitude for the 4 hour annealed device and remained constant for the 6 hour annealed device. For all devices, $I_{ON/OFF}$ improved by continuously increasing an order of magnitude for the 1, 4 and 6 hour annealed devices while V_{ON} shifted negatively. The SS remained the same and μ_{FE} increased for all devices.

Table 6

Electrical characteristics of TFTs annealed for different durations

Annealing Duration (Hr)	I_D (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/dec)	μ_{FE} ($cm^2/V \cdot s$)
1	10^{-8}	10^4	-2.5	4	0.004
6	10^{-7}	10^5	-6.2	2.4	0.02
10	10^{-7}	10^5	-9.5	2.12	0.1

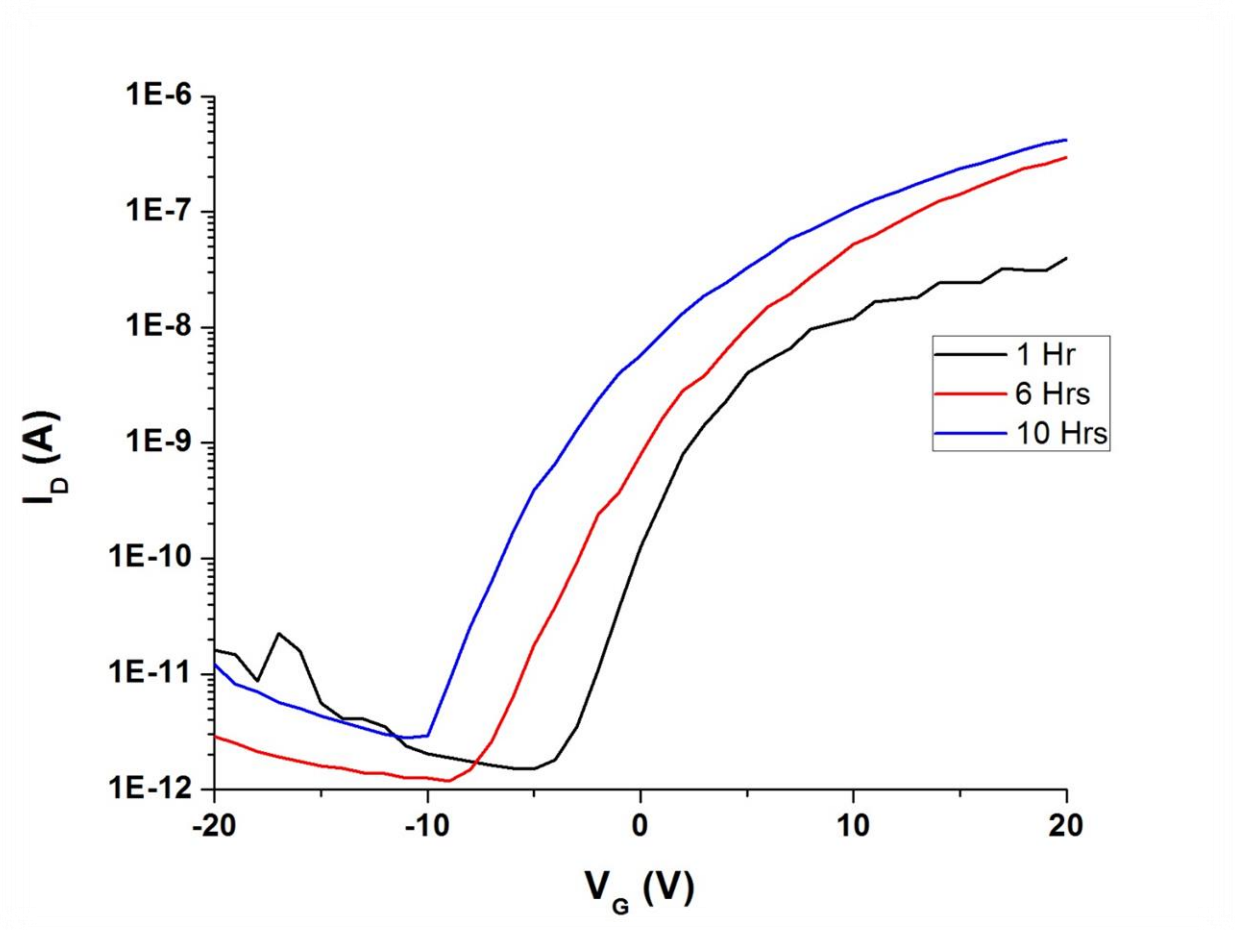

Figure 26 Transfer characteristics of TFTs annealed at 1, 6 and 10 hours in air

Table 7

The electrical properties of TFTs annealed for different durations before and after PCA

Annealing Duration (Hr)	I_{ON} (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/Dec)	μ_{FE} ($x10^{-2}$ $cm^2/V \cdot s$)
1	$1x10^{-8}$	$1x10^{5}$	-2.5-> -3.5	4->2	0.4 ->1.7
4	$1x10^{-7}$ -> $1x10^{-6}$	$1x10^{6}$	-6.2->-8	2.4->2	0.6 ->2.0
6	$1x10^{-7}$	$1x10^{6}$	-9.5-> -11.5	2.1->2	1.6 ->4.6

XPS characterization was done on the surface and 5 nm below 15 nm GSZO films annealed at 140 °C for 3 and 10 hours to examine the effect of annealing duration on atomic composition (Table 8). Table 9, Figure 27 and Figure 28 show the O 1s spectra de-convoluted into the three OI, OII and OIII peaks of different binding energies for films annealed for 3 and 10 hours. Table 10, Figure 29 and Figure 30 show the Sn relative at.% as a function of annealing duration. Annealing duration appears to have very little effect on the atomic composition of the film. The Sn^{2+} relative at.% on the surface of films increases (14.1 at.% to 39.6 at.%) with increasing annealing duration however decreases (74.6 at.% to 50.6 at.%) below the surface.

Table 8

Atomic percentage of 15 nm GSZO films annealed at 140 °C for 3 and 10 hours.

Annealing Duration	O-(Zn,Ga,Sn)	Cl	Zn	Ga	Sn
3 Hr Surface	53.6	1.0	41.1	2.2	2.2
3 Hr Sputtered	47.7	0.1	46.6	4.6	1.0
10 Hr Surface	53.6	0.8	41.7	1.9	2.0
10 Hr Sputtered	44.9	0.0	49.8	4.0	1.3

Table 9

O-1s related relative percentage of 15 nm GSZO films annealed at 140 °C for 3 and 10 hours.

Annealing Duration	O Relative %			Binding Energy (eV)		
	OI	OII	OIII	OI	OII	OIII
3 Hr Surface	61	34	5	530.2	531.7	532.7
3 Hr Sputtered	76	24	0	530.3	531.7	532.7
10 Hr Surface	59	34	6	530.3	531.7	532.7
10 Hr Sputtered	82	18	0	530.1	531.5	532.7

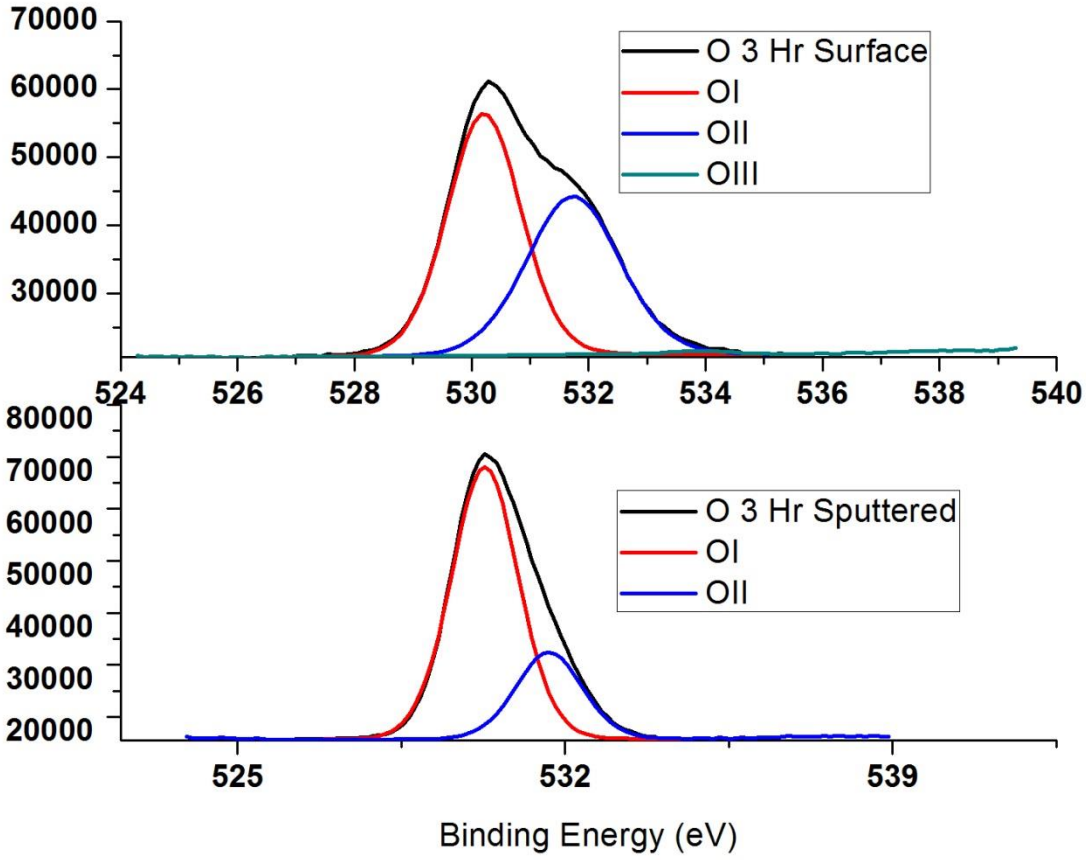

Figure 27 XPS spectra of O ions in GSZO films annealed at 140 °C for 3 hours.

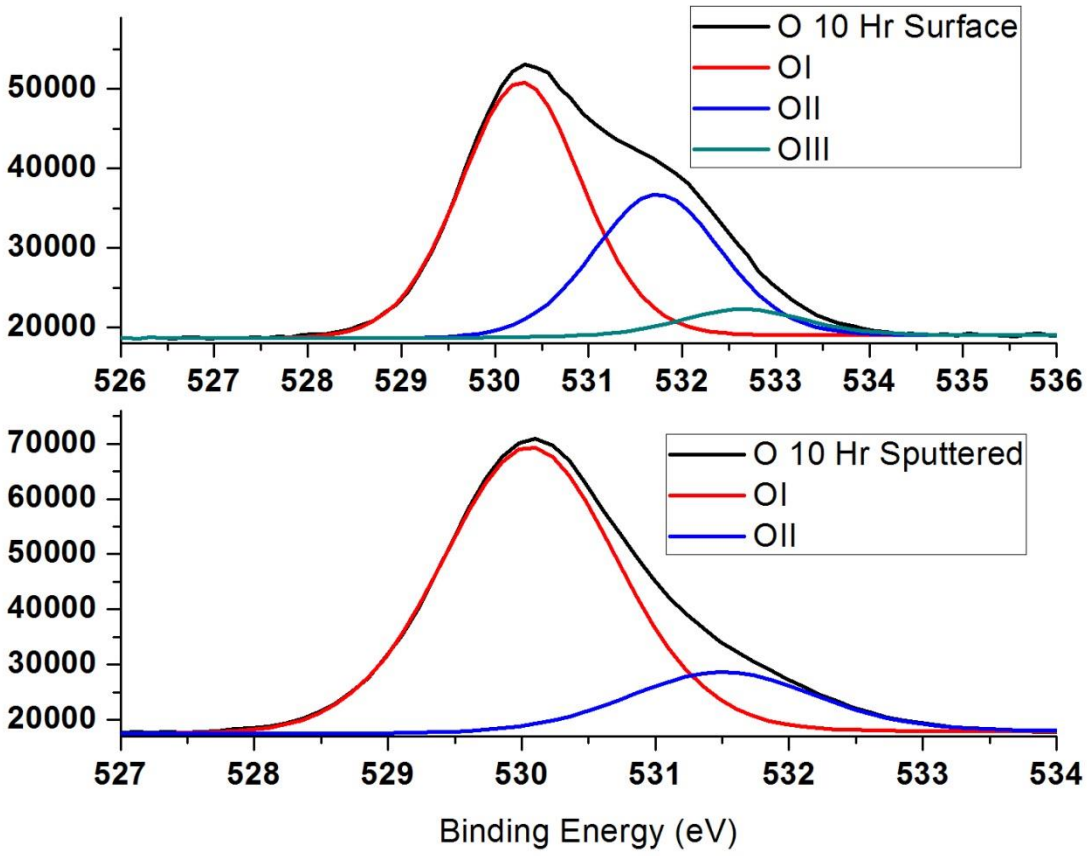

Figure 28 XPS spectra of O ions in GSZO films annealed at 140 °C for 10 hours.

Table 10

Sn related relative percentage of 15 nm GSZO films annealed at 140 °C for 3 and 10 hours.

Annealing Duration	Sn Relative%			Binding Energy (eV)		
	Sn^{2+}	Sn^{4+}	Sn^{0}	Sn^{2+}	Sn^{4+}	Sn^{0}
3 Hr Surface	14.1	85.9	0	486.2	486.8	0
3 Hr Sputtered	74.6	25.4	11.9	486.3	487.1	484.5
10 Hr Surface	39.6	60.4	0	486.3	486.8	0
10 Hr Sputtered	50.6	41.8	7.6	486	486.6	484.6

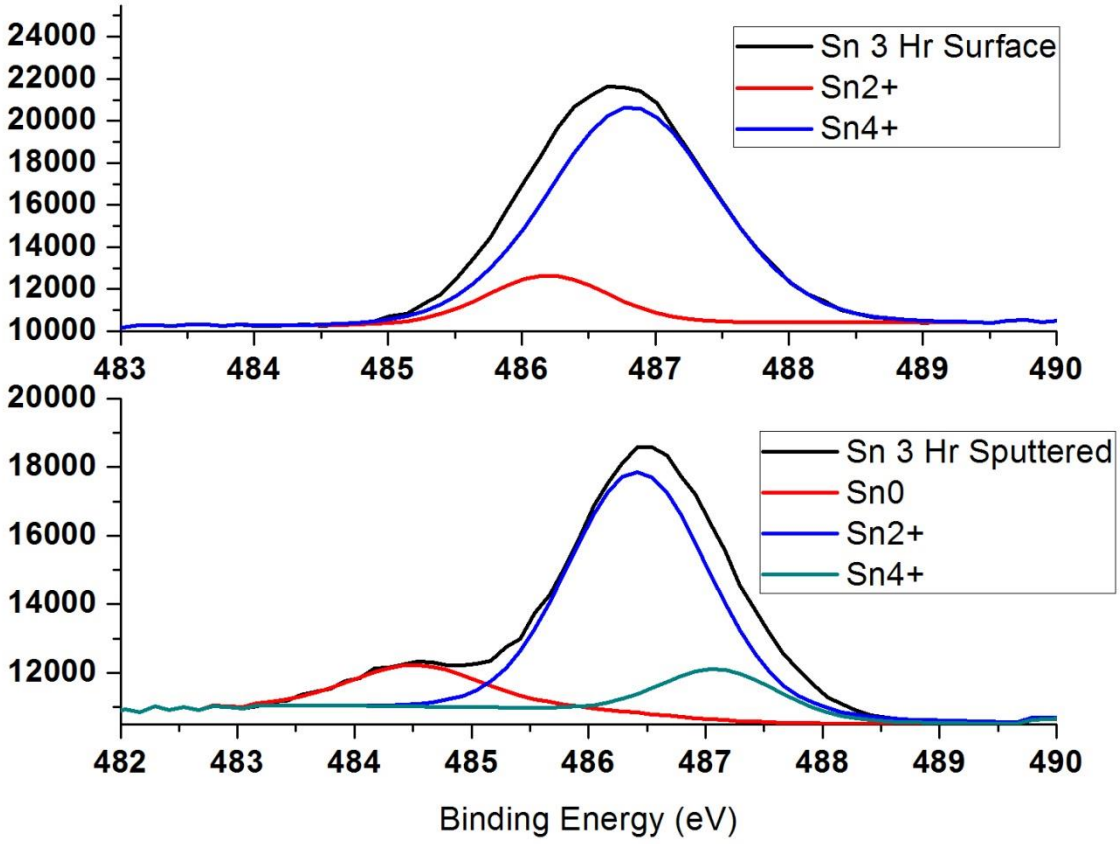

Figure 29 XPS spectra of Sn ions in GSZO films annealed at 140 °C 3 hours.

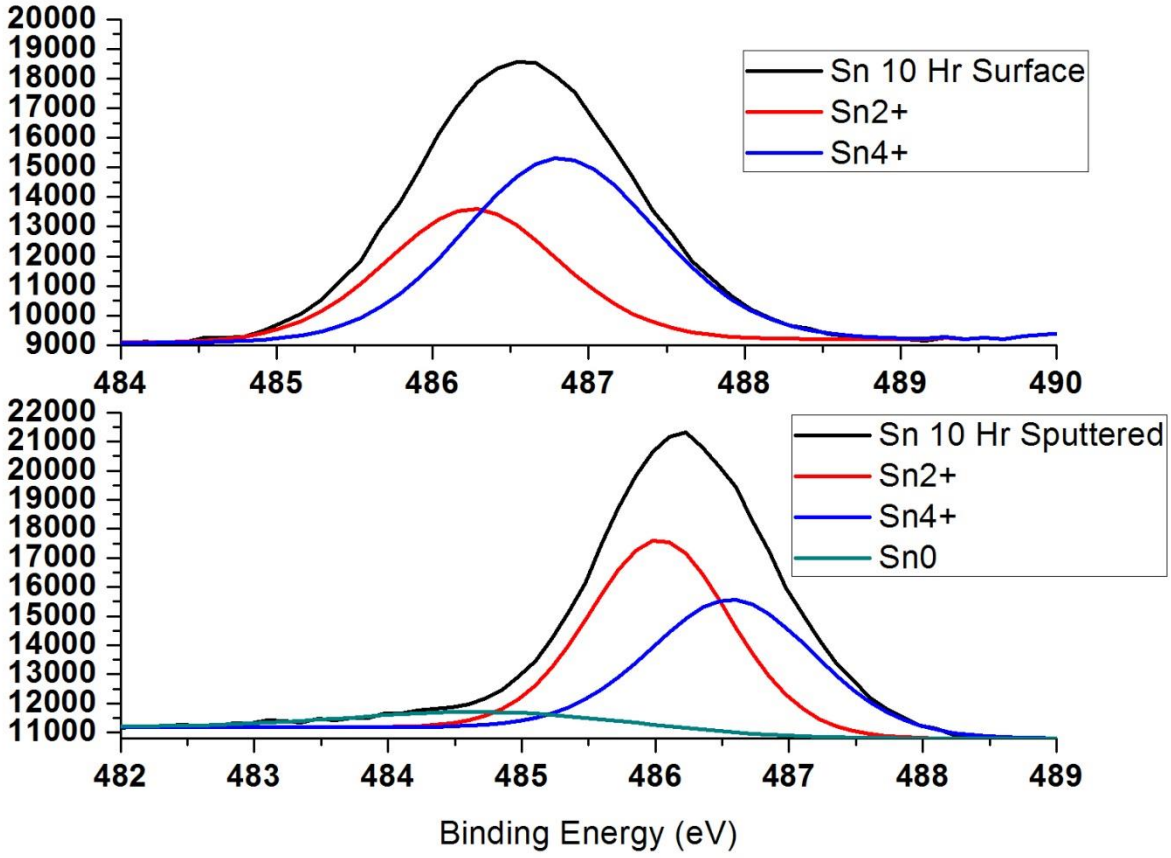

Figure 30 XPS spectra of Sn ions in GSZO films annealed at 140 °C for 10 hours.

5.3 Deposition Temperature

The deposition temperature was increased from 50 °C to 100 °C to examine its effects on the electrical performance of the TFTs which are shown in Table 11 and displayed in Figure 31. The maximum drain current I_D increased an order of magnitude and $I_{ON/OFF}$ improved by two orders of magnitude with increasing deposition temperature. V_{ON} shifted negatively from -3.2 V to -7 V while the SS slightly degraded by 0.7 V/dec.

Table 11

Electrical characteristics of TFTs deposited at different temperatures

Deposition Temperature (°C)	I_D (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/Dec)
50	10^{-8}	10^3	-3.2	2
100	10^{-7}	10^5	-7	2.7

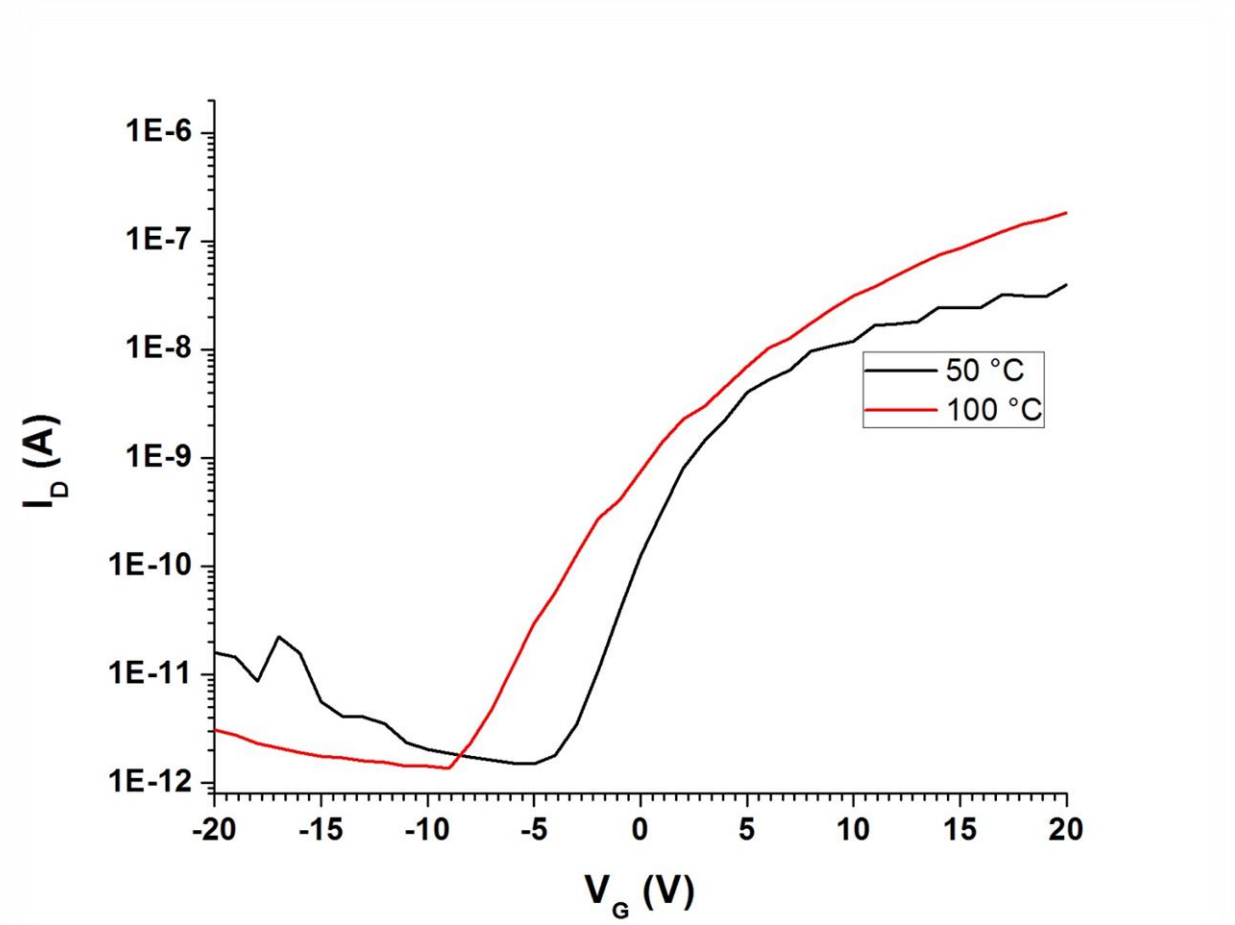

Figure 31 Transfer graphs of TFTs with varying deposition temperatures.

XPS characterization was done on the surface and 5 nm below 15 nm GSZO films deposited at 50 °C and 100 °C examine the effect of deposition temperature on atomic composition (Table

12). Table 13 and *Figure 32* and *Figure 33* show the O-1s spectra de-convoluted into the three OI, OII and OIII peaks of different binding energies for films deposited at 50 °C and 100 °C. Table 14 and Figure 34 and Figure 35 show the Sn relative at.% as a function of annealing duration. Increasing deposition temperature appear to decrease the O-1s and increase the Zn related atomic concentration on the surface however there appear to be little change below the surface. Deposition temperature appears to have little effect on the OI and OII species however traces of OIII related species can be found within the bulk of the 50 °C deposited film. The surface of both films contains a large concentration of Sn^{4+} while the bulk of the films are mostly Sn^{2+}. The 100 °C deposited film contains higher concentrations of Sn^{4+} in the bulk than the 50 °C deposited film and traces of Sn^{0} can also be found.

Table 12

Atomic percentage of 15 nm GSZO films deposited at 50 °C and 100 °C.

Deposition Temperature	O-(Zn,Ga,Sn)	Cl	Zn	Ga	Sn
50 °C Surface	59.2	0.4	36.6	1.6	2.1
50 °C Sputtered	46.4	0.0	48.5	3.8	1.3
100 °C Surface	53.6	1.0	41.1	2.2	2.2
100 °C Sputtered	47.7	0.1	46.6	4.6	1.0

Table 13

O-1s related relative percentage of 15 nm GSZO films deposited at 50 °C and 100 °C.

Deposition Temperature	O Relative %			Binding Energy (eV)		
	OI	OII	OIII	OI	OII	OIII
50 °C Surface	54	39	7	530.4	531.8	532.7
50 °C Sputtered	78	21	1	530.2	531.6	532.7
100 °C Surface	61	34	5	530.2	531.7	532.7
100 °C Sputtered	76	24	0	530.3	531.7	532.7

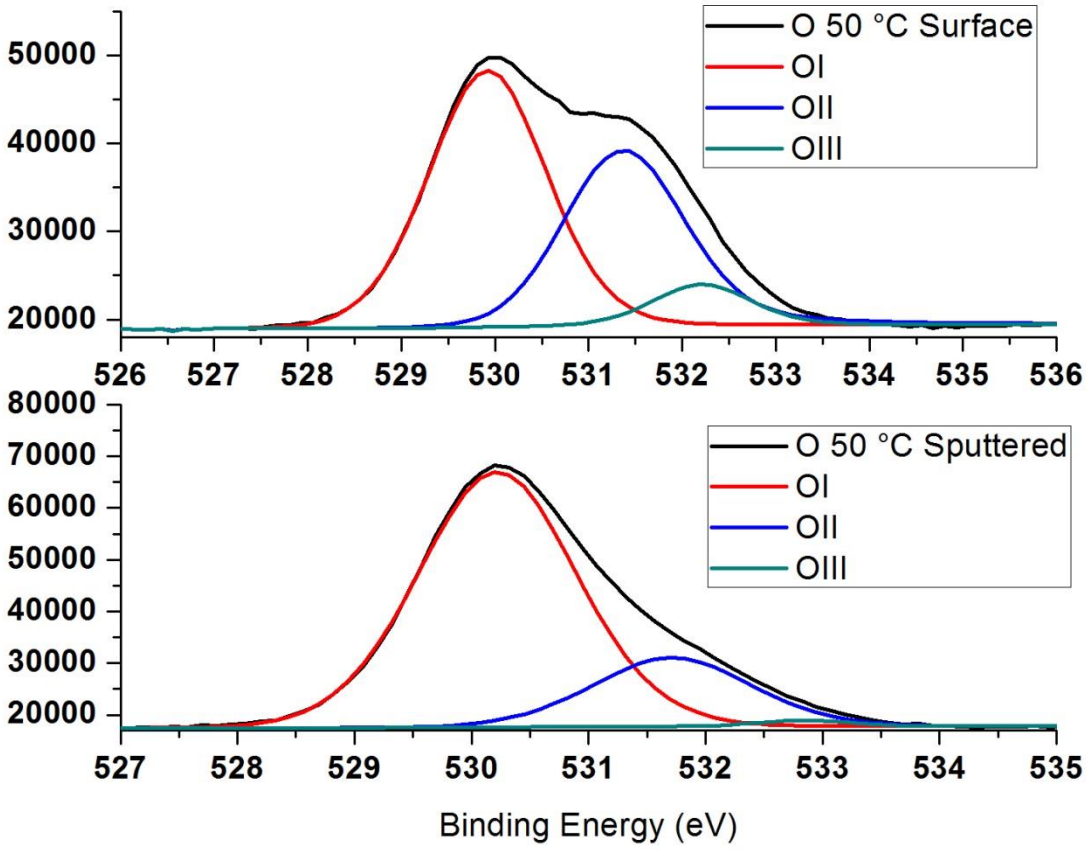

Figure 32 XPS spectra of O ions in GSZO films deposited at 50 °C.

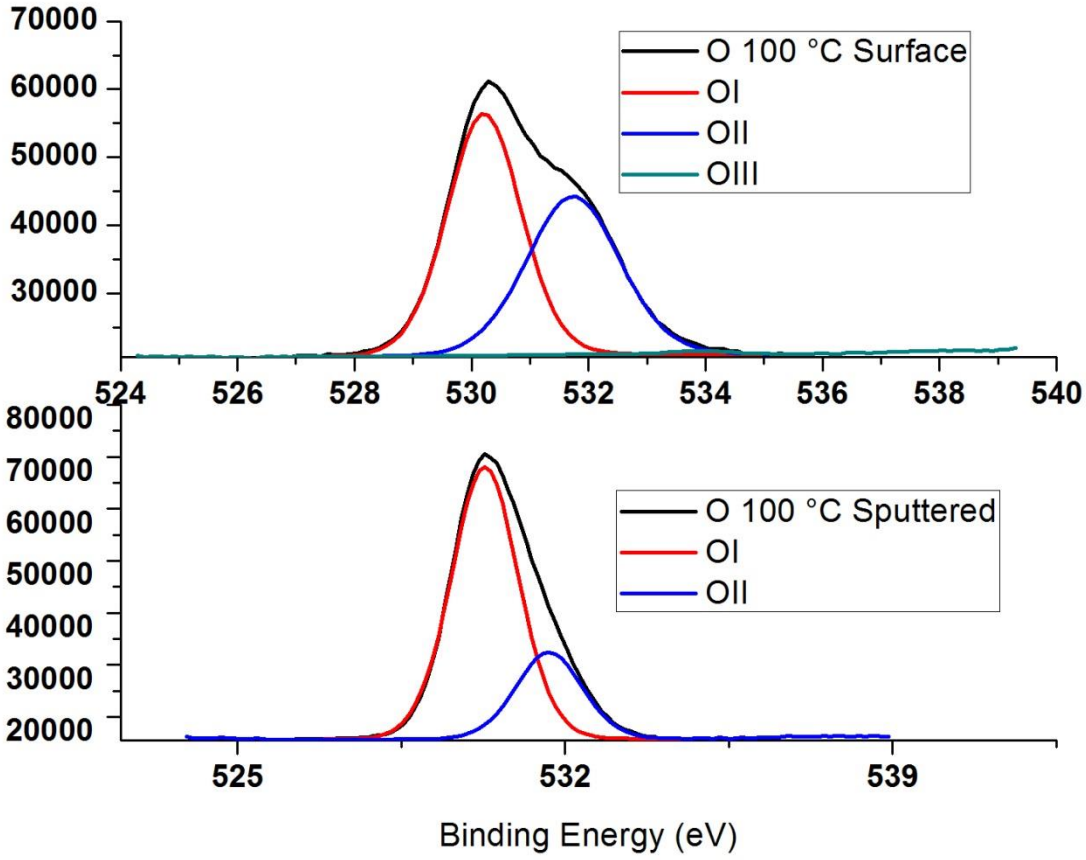

Figure 33 XPS spectra of O ions in GSZO films deposited at 100 °C.

Table 14

Sn related relative percentage of 15 nm GSZO films deposited at 50 °C and 100 °C.

Deposition Temperature	Sn Relative%			Binding Energy (eV)		
	Sn^{2+}	Sn^{4+}	Sn^{0}	Sn^{2+}	Sn^{4+}	Sn^{0}
50 °C Surface	25.2	74.8	0	486.2	486.8	0
50 °C Sputtered	84.4	15.6	0	486.2	486.8	485.7
100 °C Surface	14.1	85.9	0	486.2	486.8	0
100 °C Sputtered	74.6	25.4	11.9	486.3	487.1	484.5

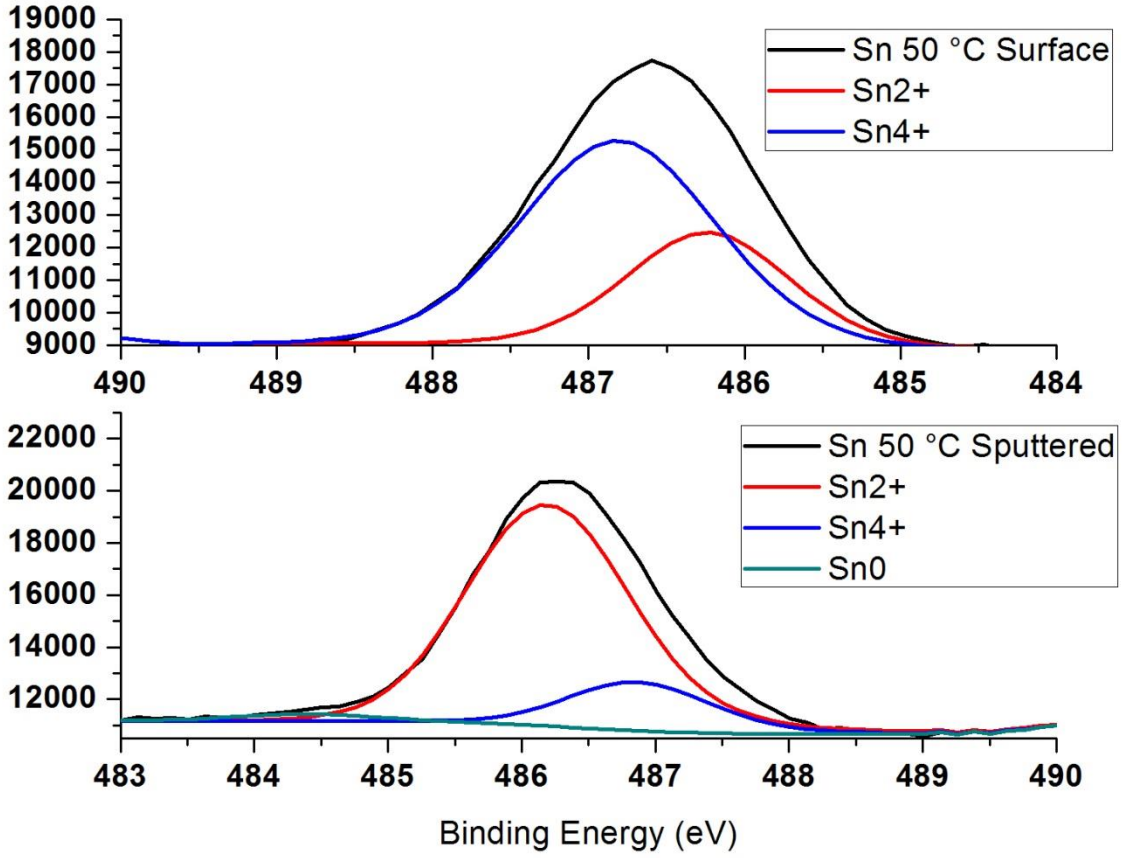

Figure 34 XPS spectra of Sn ions in GSZO films deposited at 50 °C.

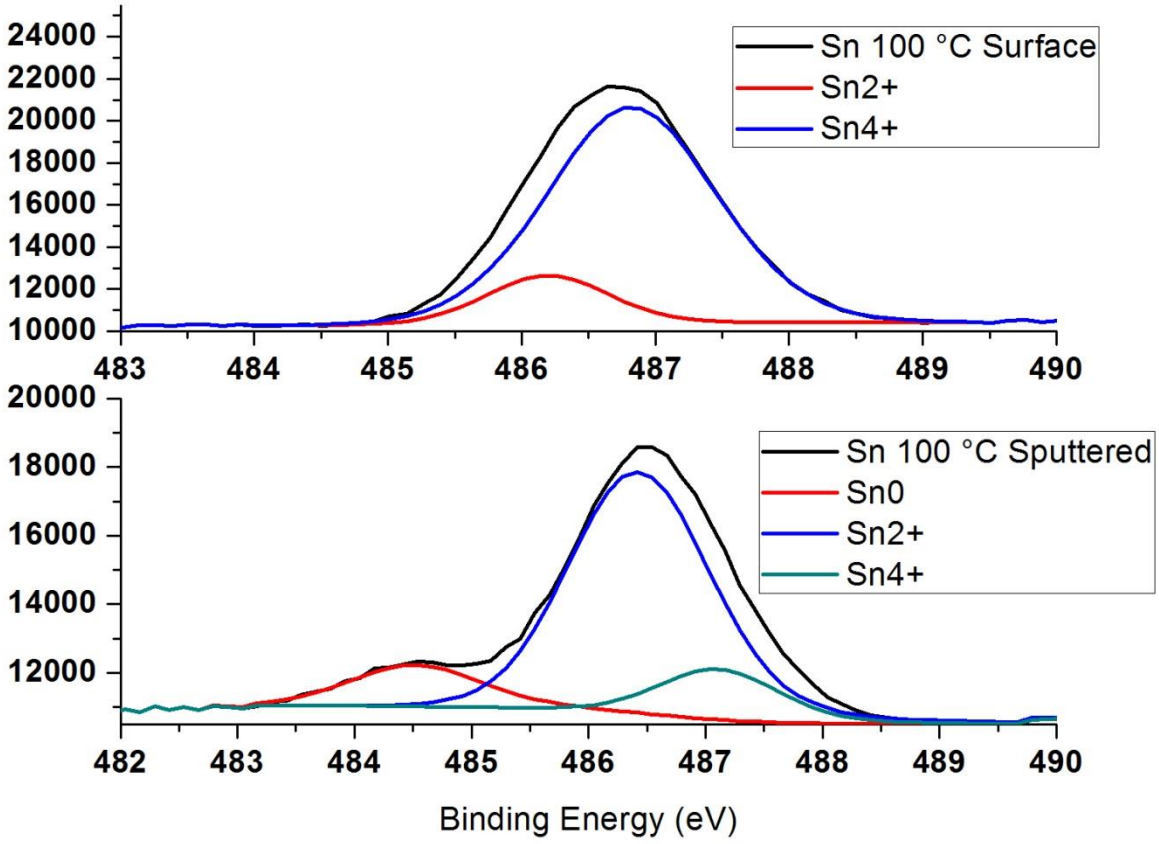

Figure 35 XPS spectra of Sn ions in GSZO films deposited at 100 °C.

5.4 Channel Thickness

Active layer thicknesses were varied to examine its effect on the electrical properties of the devices. I-V properties of 30, 20, 15 and 10 nm are displayed in Table 15 and Figure 36 along with C-V properties shown in Figure 37. XRR characterizations were also taken on devices with decreasing channel thickness and are also shown in Table 15. Both I_{ON} and I_{OFF} decrease with decreasing channel thickness, with $I_{ON/OFF}$ remaining invariant in the 10^6 range from 30 nm to 10 nm. V_{ON} is largely negative at 30 nm however it shifts positively to -5 V at 15 and 10 nm. SS also improves from 2.1 to 1.06 V/dec with reduction in channel thickness with a corresponding increase in μ_{FE} to 0.14 $cm^2/V \cdot s$. The C-V graph shows no depletion region and

small slope for the 30 nm device with a corresponding increase in slope with decreasing channel thickness. XRR measurements reveal an increase in film density (5.5, 5.9 and 6.5 g/cm^3) with decreasing channel thickness for 30, 15 and 10 nm, respectively. RBS characterization was carried out on 23 nm and 13 nm films and the results are shown in Table 16, Figure 38 and Figure 39. Both results show that film composition is invariant with increasing film thickness.

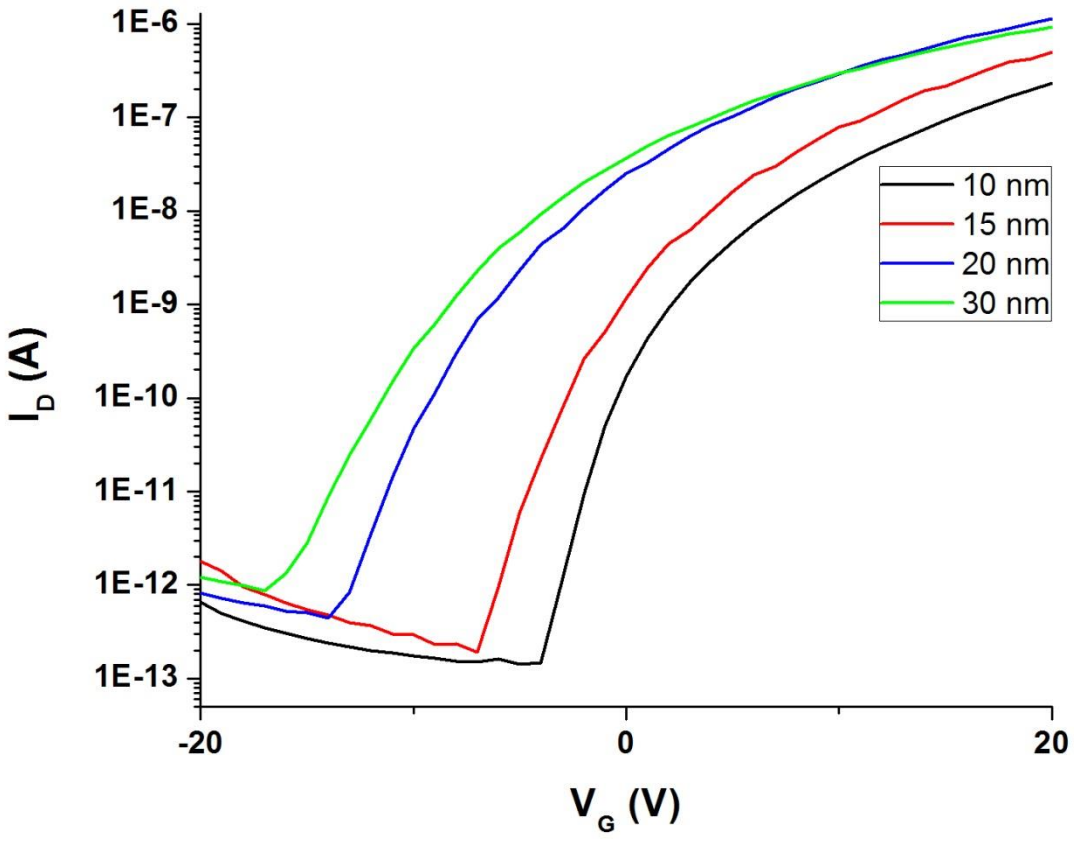

Figure 36 Transfer graph of TFTs with different thicknesses.

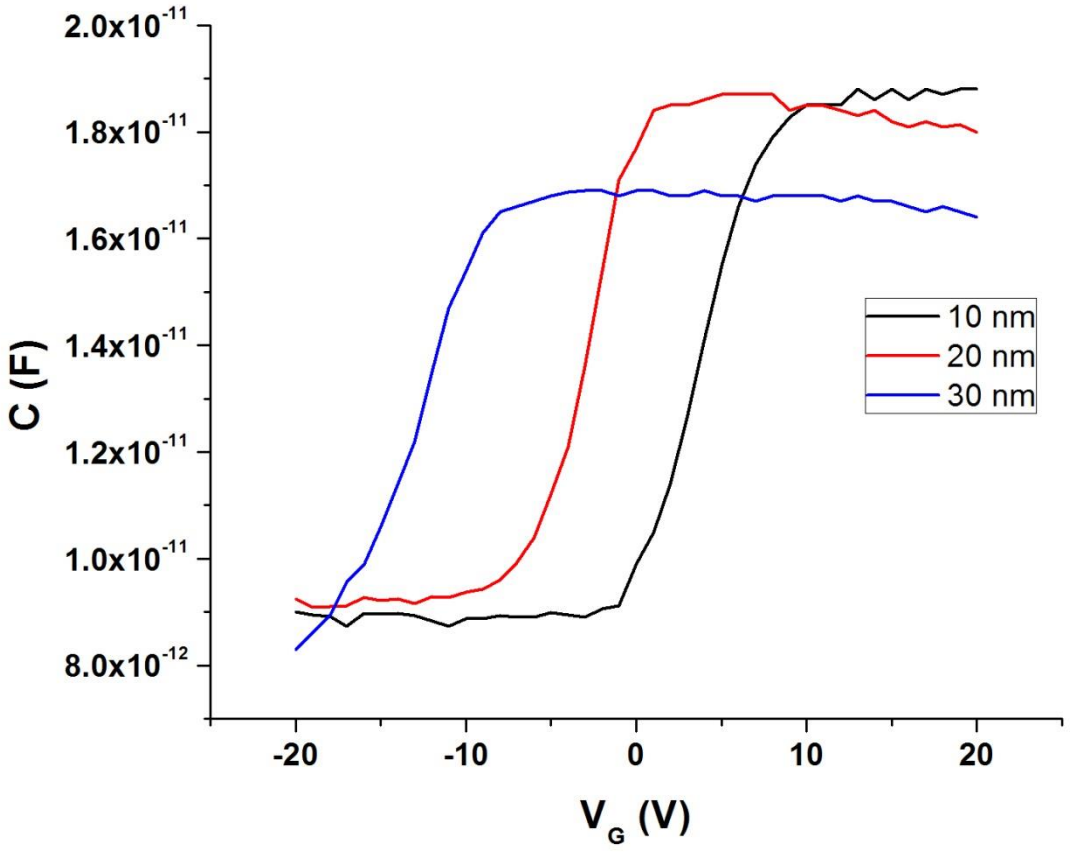

Figure 37 C-V graph of TFTs with different thicknesses.

Table 15

Electrical characteristics of TFTs with different thicknesses

Channel Thickness (nm)	I_D (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/dec)	μ_{FE} ($cm^2/V \cdot s$)	Density (g/cm^3)
30	$9x10^{-7}$	$1x10^6$	-14.5	2.1	N/A	5.5
20	$1x10^{-6}$	$2x10^6$	-12	1.6	0.07	N/A
15	$5x10^{-7}$	$3x10^6$	-5	1.3	0.07	5.9
10	$3x10^{-7}$	$1x10^6$	-5	1.06	0.14	6.5

Table 16

RBS characterization of films with different thicknesses.

Thickness (nm)	Atomic Concentrations (at%)				Density (at/cc)
	Ga	Zn	O	Sn	
13	2.9	40.8	54.6	1.7	$6.77x10^{22}$
23	3.1	43.1	52	1.8	$6.75x10^{22}$

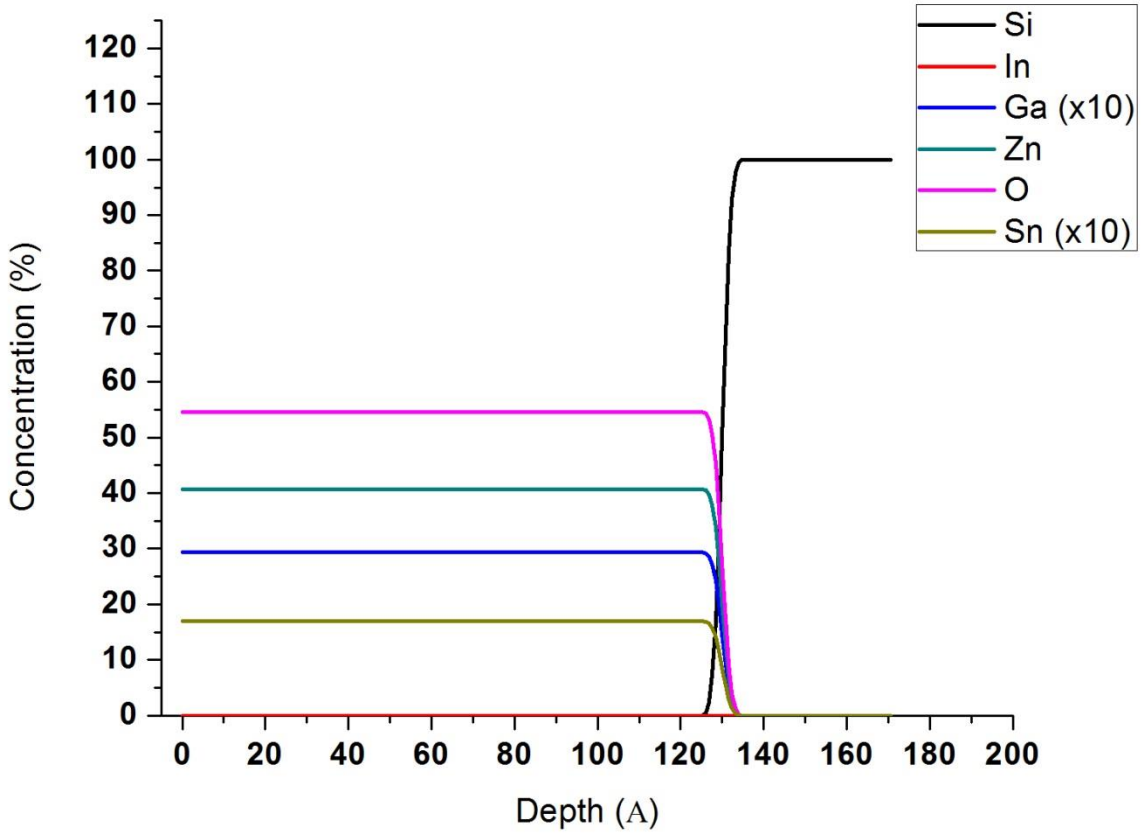

Figure 38 RBS plot of 13 nm GSZO film

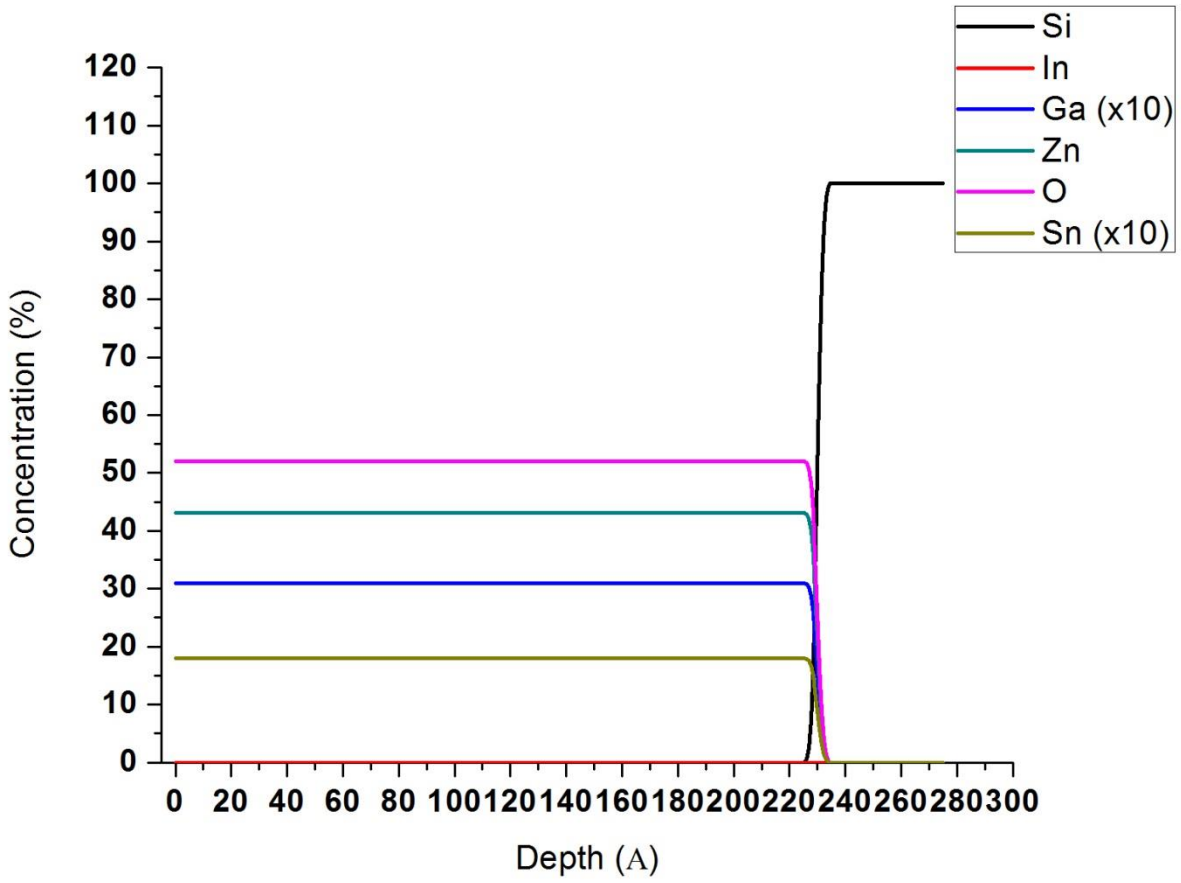

Figure 39 RBS plot of 23 nm GSZO film

The PCA procedure was used in attempt to further improve the performance of the devices with different channel thicknesses. The electrical performance is shown in Table 17 and *Figure 40-Figure 42*. The $I_{ON/OFF}$ decreased nearly by an order of magnitude due to an increase in I_{OFF} while V_{ON} shifted negatively beyond -25 V for the 30 nm device. The 20 nm and 10 nm devices exhibited an increase in $I_{ON/OFF}$ and a positive shift in V_{ON}. The SS increased slightly for the 30 nm device, remained constant for the 20 nm device and decreased slightly for the 10 nm device. The μ_{FE} increased slightly for the 20 nm device and remained constant for the 10 nm device.

Table 17

The electrical properties of TFTs with various channel thicknesses before and after PCA

Film Thickness	I_{ON}	I_{OFF}	$I_{ON/OFF}$	V_{ON}	SS	μ_{FE}
30 nm	$6x10^{-7}$ ->$2x10^{-6}$	$9 x10^{-13}$ ->$1x10^{-11}$	$7 x10^{5}$ ->$1 x10^{5}$	-14.5 ->Beyond -25	3.0->3.2	-
20 nm	$6x10^{-7}$ ->$5x10^{-7}$	$4 x10^{-13}$ ->$2x10^{-13}$	$2 x10^{6}$ ->$3 x10^{6}$	-11.8 ->-8.8	1.8	.01 ->.08
10 nm	$3x10^{-7}$ ->$9x10^{-7}$	$1x10^{-13}$ ->$6x10^{-14}$	$3x10^{6}$ ->$2x10^{7}$	-5->-3.4	1.1->.96	0.14

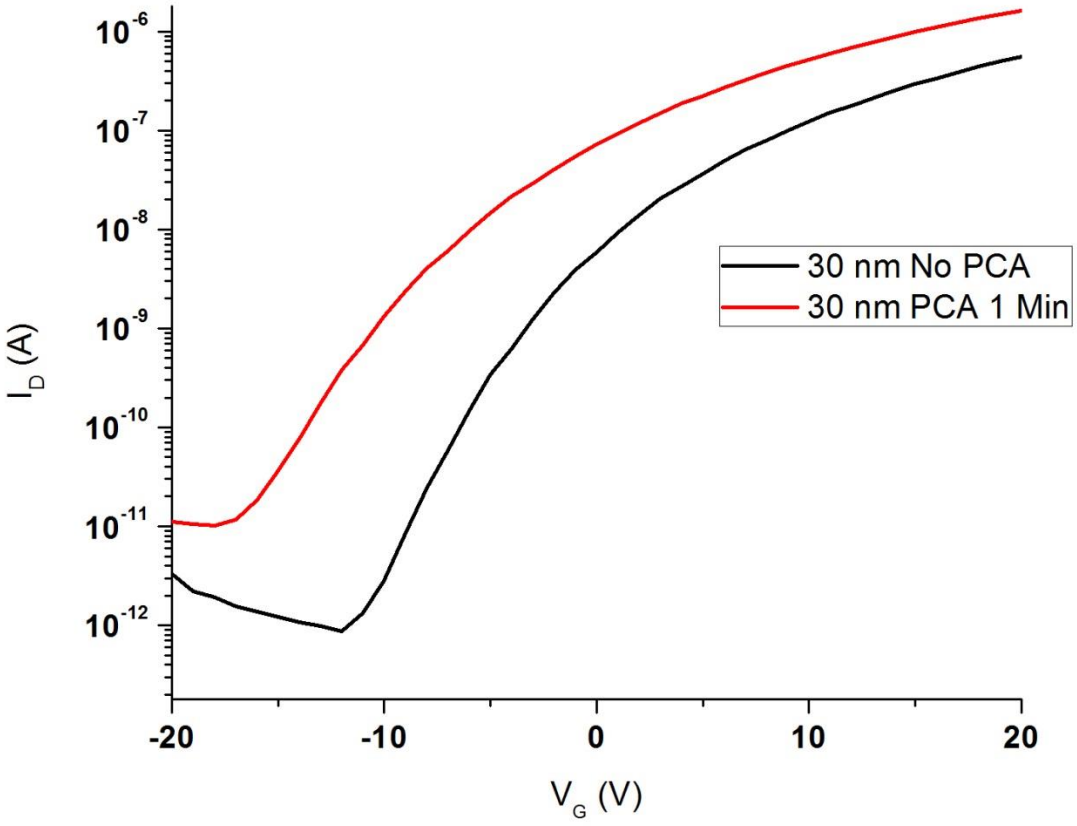

Figure 40 Effect of post-contact annealing on TFTs with 30 nm GSZO channel layer

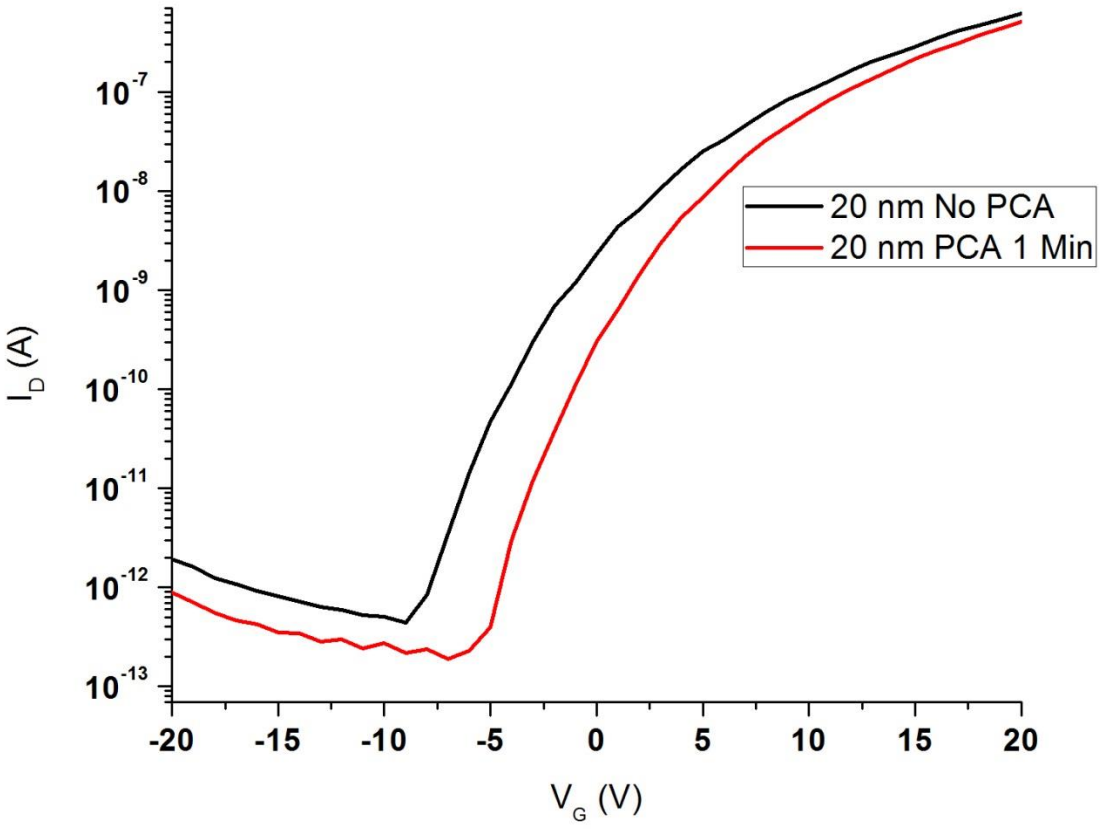

Figure 41 Effect of post-contact annealing on TFTs with 20 nm GSZO channel layer

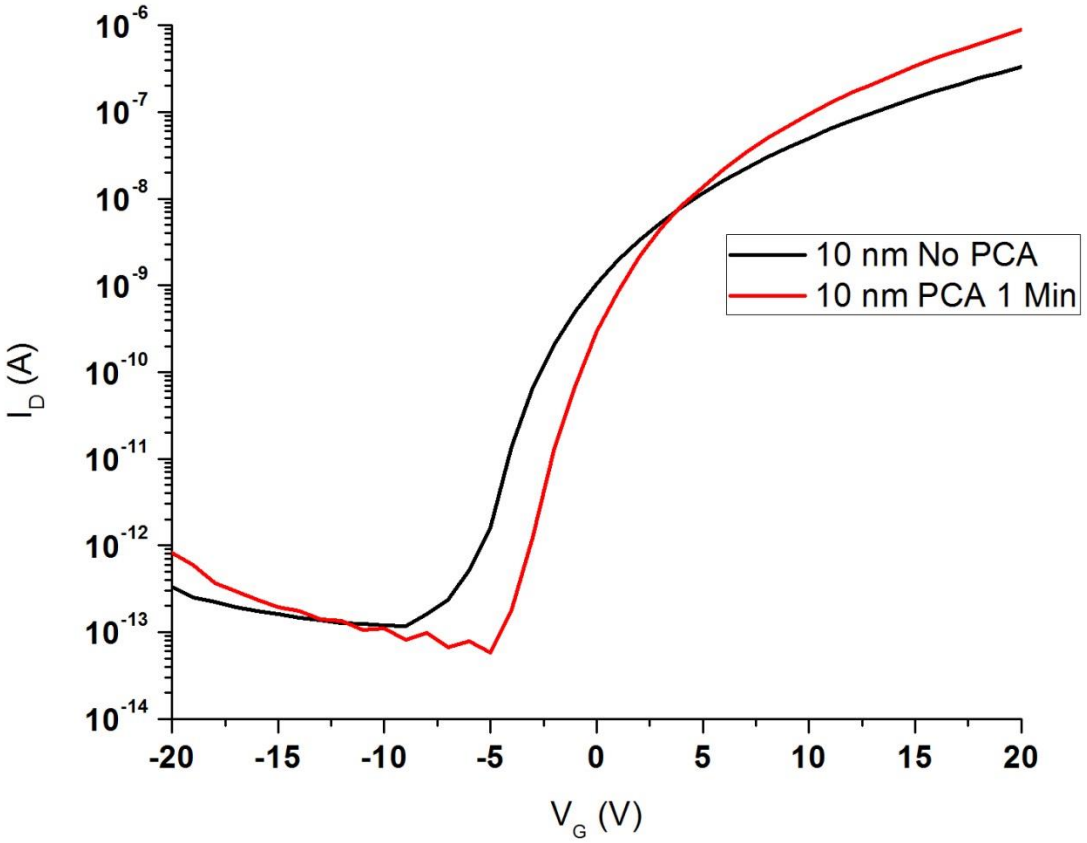

Figure 42 Effect of post-contact annealing on TFTs with 10 nm GSZO channel layer

5.5 Higher Annealing Temperature

Further examining on the effects of annealing temperature was taken to investigate the effect of high annealing temperatures. A GSZO TFT annealed at 140 °C for 3 hours and 450 °C for 1 hour were fabricated and the I-V plots are shown in Figure 43 and Table 18. It can be seen that overall device performance improves with increasing annealing temperature. SS 1.1 V/dec to 0.4 V/dec, I_{ON} increased 2 orders of magnitude and $I_{ON/OFF}$ increased 3 orders of magnitude. XPS characterization was taken on the above films to examine the effect of annealing temperature on atomic composition (Table 19). Both films are more O-rich on the surface however the 450 °C film contains is slightly more O-rich than the 140 °C annealed film. While the O at.% and Zn

at.% is roughly the same in the bulk of the 140 °C annealed film the 450 °C annealed film shows a large increase in Zn at.%. An increase in Ga at.% and decrease in Sn at.% can be seen in the bulk of both samples however the difference between the samples remain invariant. Table 20 and Figure 44 and Figure 45 show the O-1s spectra de-convoluted into three peaks of different states, i.e., 530.2 eV (OI), 531.7 eV (OII) and 532.7 eV (OIII) for films annealed at 140 °C and 450 °C. On the surface, both films exhibit nearly the same at.% however a difference between the films can be seen 5 nm below the surface. The relative OI at.% increases and OII at.% decreases by 10 % with increasing annealing temperature while the presence of OIII related O-1s elements vanish within the bulk. Table 21 and Figure 46 and Figure 47 show the Sn relative at.% for films annealed at 140 °C and 450 °C. The surface of both films is majority Sn^{4+} however a difference can be seen within the bulk. The 140 °C annealed film showed a ~60 % decrease in Sn^{4+} below the surface while the 450 °C showed only a 14 % decrease. The 140 °C annealed film also showed traces of the metal Sn^{0} on the surface however these traces were not found within the bulk and the 450 °C annealed film showed no traces of Sn^{0} neither on the surface nor within the bulk.

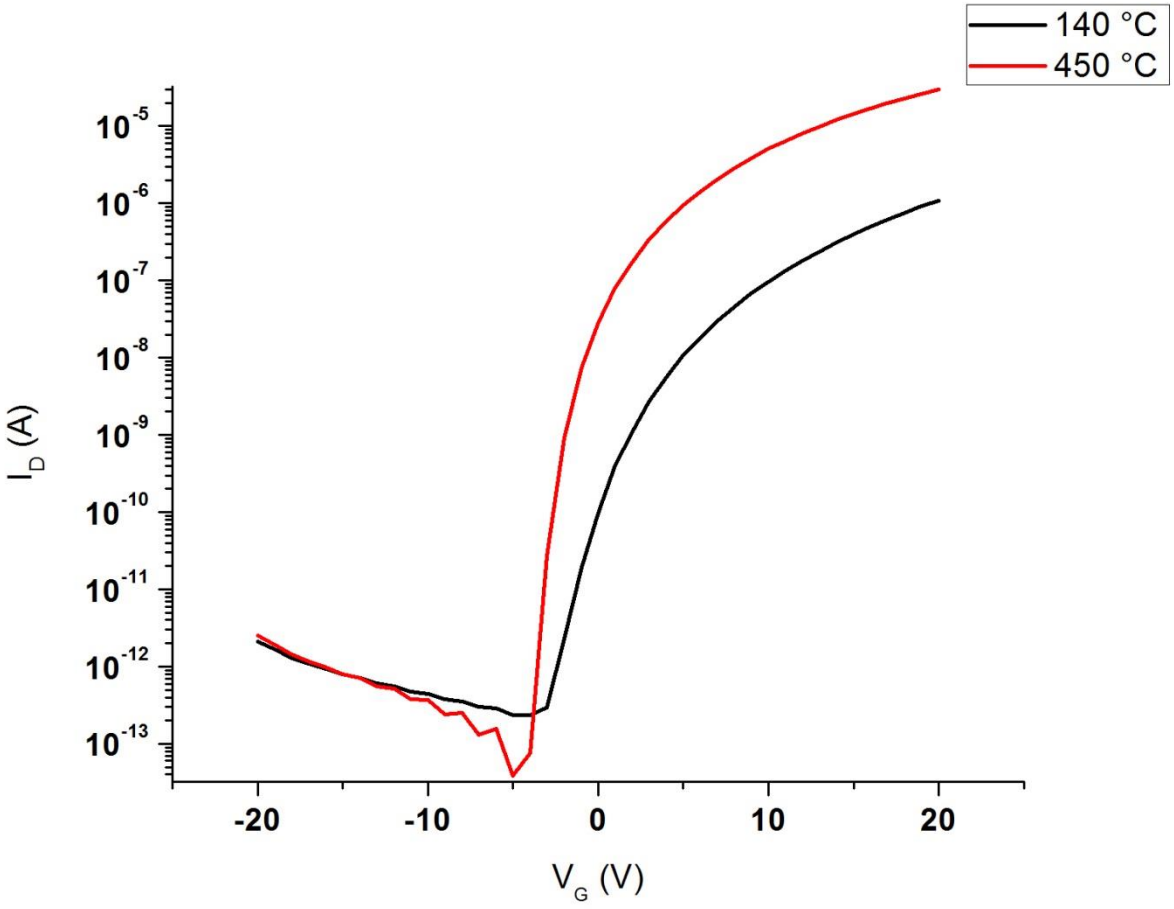

Figure 43 I-V transfer curves of GSZO TFTs annealed at 140 °C for 3 hours and 450 °C for 1 hour.

Table 18

Electrical characteristics of TFTs annealed at 140 °C for 3 hours and 450 °C for 1 hour.

Annealing Temperature	I_{ON} (A)	$I_{ON/OFF}$	V_{ON} (V)	SS (V/dec)
140 °C	10^{-7}	10^{6}	-2	1.1
450 °C	10^{-5}	10^{9}	-3.5	0.4

Table 19

Atomic percentage of 15 nm GSZO films annealed at 140 °C for 3 hours and 450 °C for 1 hour.

Annealing Temperature	O-(Zn,Ga,Sn)	Cl	Zn	Ga	Sn
140 °C Surface	53.6	1.0	41.1	2.2	2.2
140 °C Sputtered	47.7	0.1	46.6	4.6	1.0
450 °C Surface	58.7	0.3	37.0	1.6	2.3
450 °C Sputtered	43.6	0.0	50.8	4.3	1.3

Table 20

O-1s related relative percentage of 15 nm GSZO films annealed at 140 °C for 3 hours and 450 °C for 1 hour.

Annealing Temperature	O Relative %			Binding Energy (eV)		
	OI	OII	OIII	OI	OII	OIII
140 °C Surface	61	34	5	530.2	531.7	532.7
140 °C Sputtered	76	24	0	530.3	531.7	532.7
450 °C Surface	58	35	7	530.3	531.8	532.7
450 °C Sputtered	86	14	0	530.3	531.7	532.7

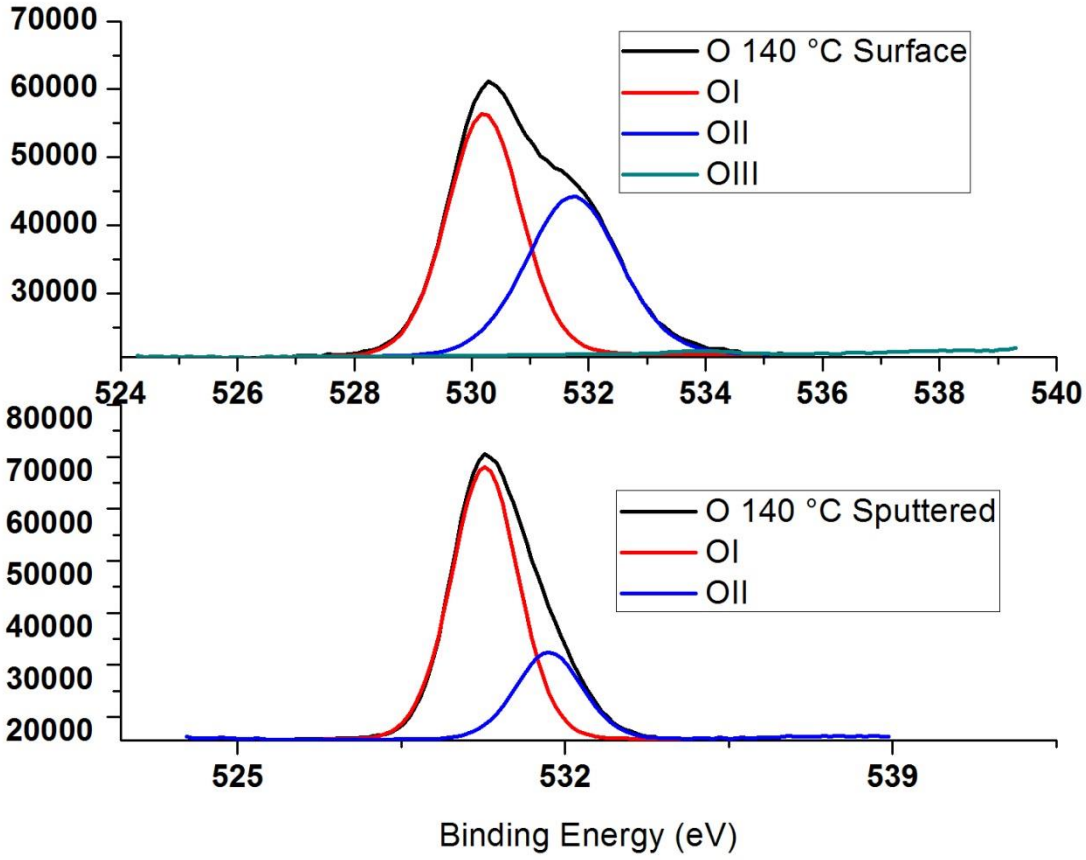

Figure 44 XPS spectra of O ions in GSZO films annealed at 140 °C for 3 hours.

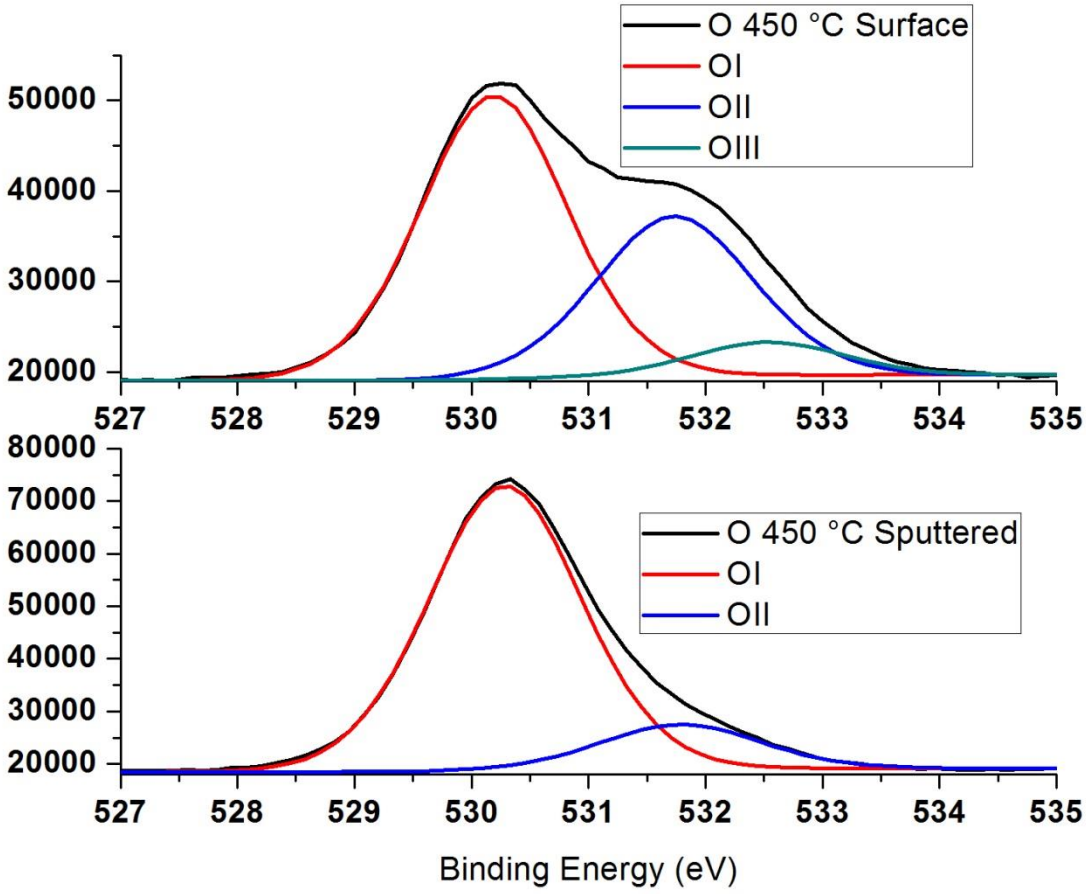

Figure 45 XPS spectra of O ions in GSZO films annealed at 450 °C for 1 hour.

Table 21

Sn related relative percentage of 15 nm GSZO films annealed at 140 °C for 3 hours and 450 °C for 1 hour.

Annealing Temperature	Sn Relative%			Binding Energy (eV)		
	Sn^{2+}	Sn^{4+}	Sn^{0}	Sn^{2+}	Sn^{4+}	Sn^{0}
140 °C Surface	14.1	85.9	0	486.2	486.8	0
140 °C Sputtered	74.6	25.4	11.9	486.3	487.1	484.5
450 °C Surface	28.1	71.9	0	486.2	486.8	0
450 °C Sputtered	42.6	57.4	0	486.2	486.8	0

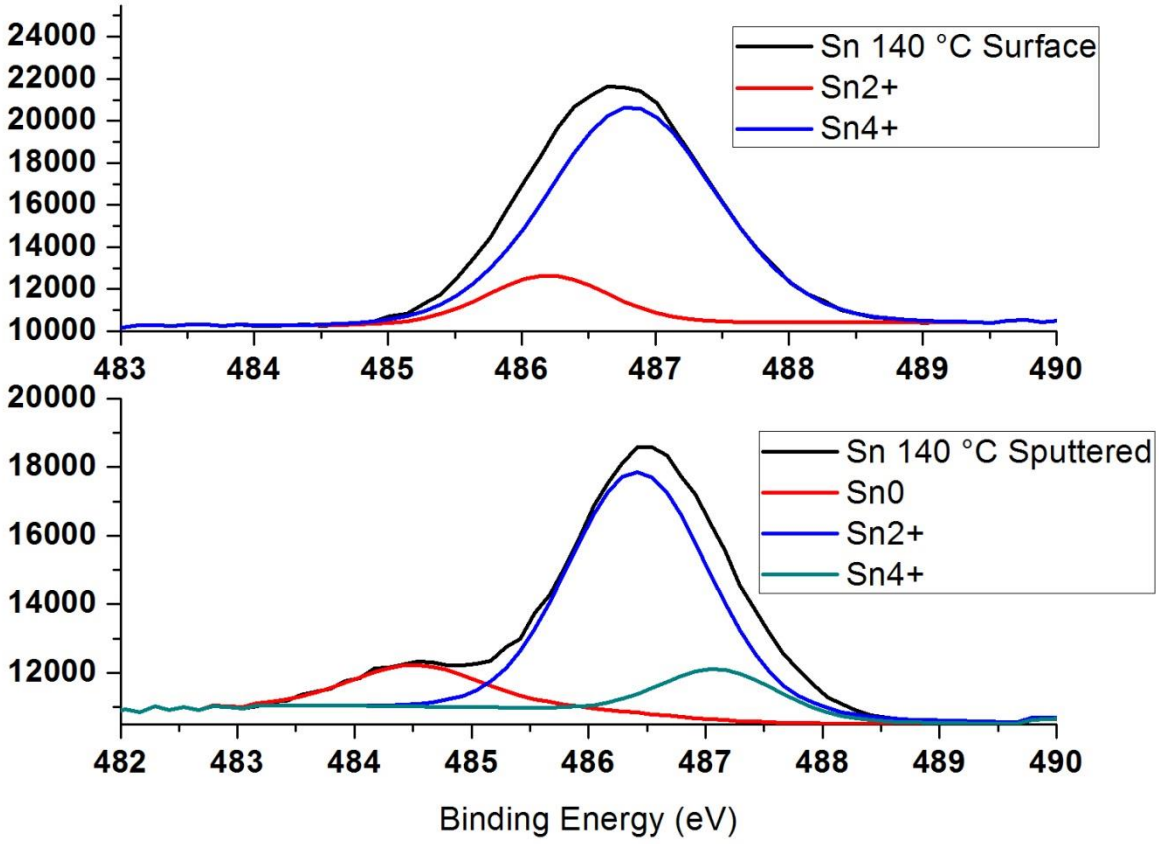

Figure 46 XPS spectra of Sn ions in GSZO films annealed at 140 °C 3 hours.

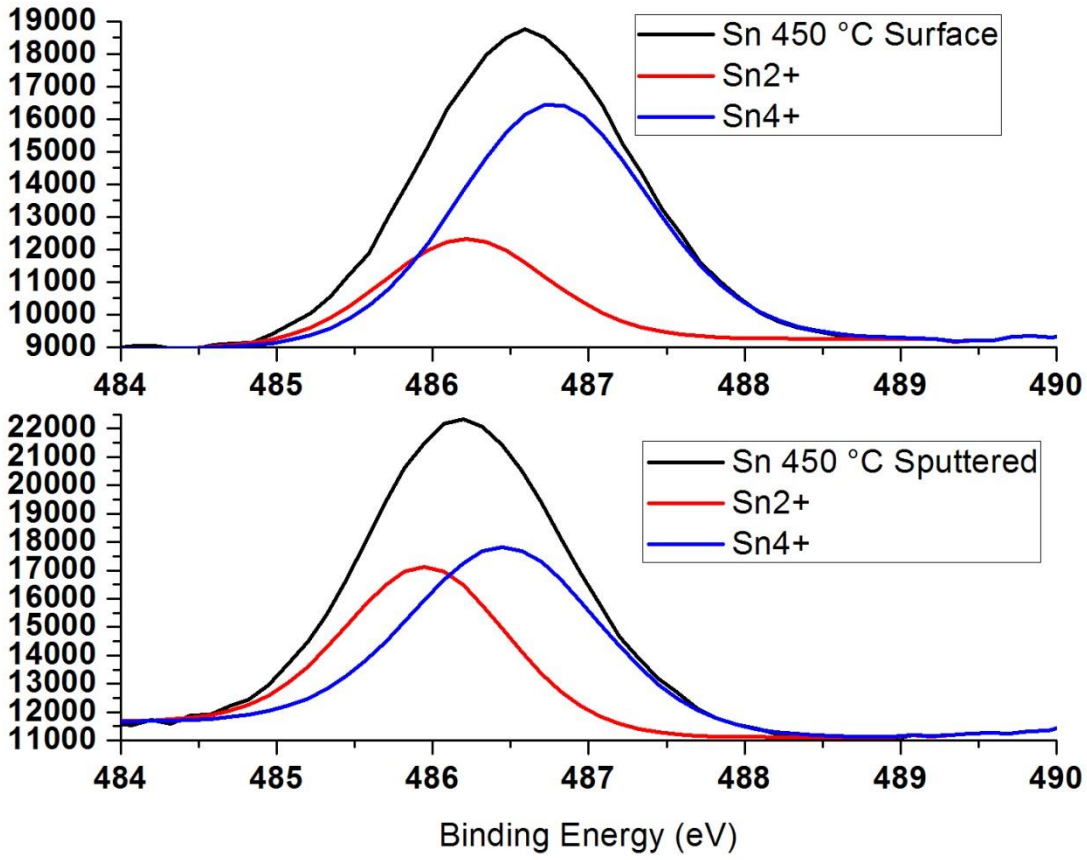

Figure 47 XPS spectra of Sn ions in GSZO films annealed at 450 °C for 1 hour.

5.6 Hysteresis

Hysteresis measurements were taken to observe the switching stability of the devices as a function of annealing duration. TFTs with 10 nm GSZO channels were annealed for either 3, 1, or 0 hours in air. For these devices, V_{ON} is the voltage at which $I_D = 10^{-10}$ A with the change in V_{ON} shown and electrical characteristics presented in Figure 48 and Table 22. It can be seen that the area between the forward and reverse I-V transfer curves reduces as annealing duration increases with ΔV_{ON} decreasing from 5-0.9 V. Along with a reduction in hysteresis is the absence of ridges in the I-V curves resulting in smoother curves as annealing duration increases.

Table 22

Change in ΔV_{ON} as annealing duration increases.

Annealing Duration (Hr)	ΔV_{ON}
0	5
1	1.1
3	0.9

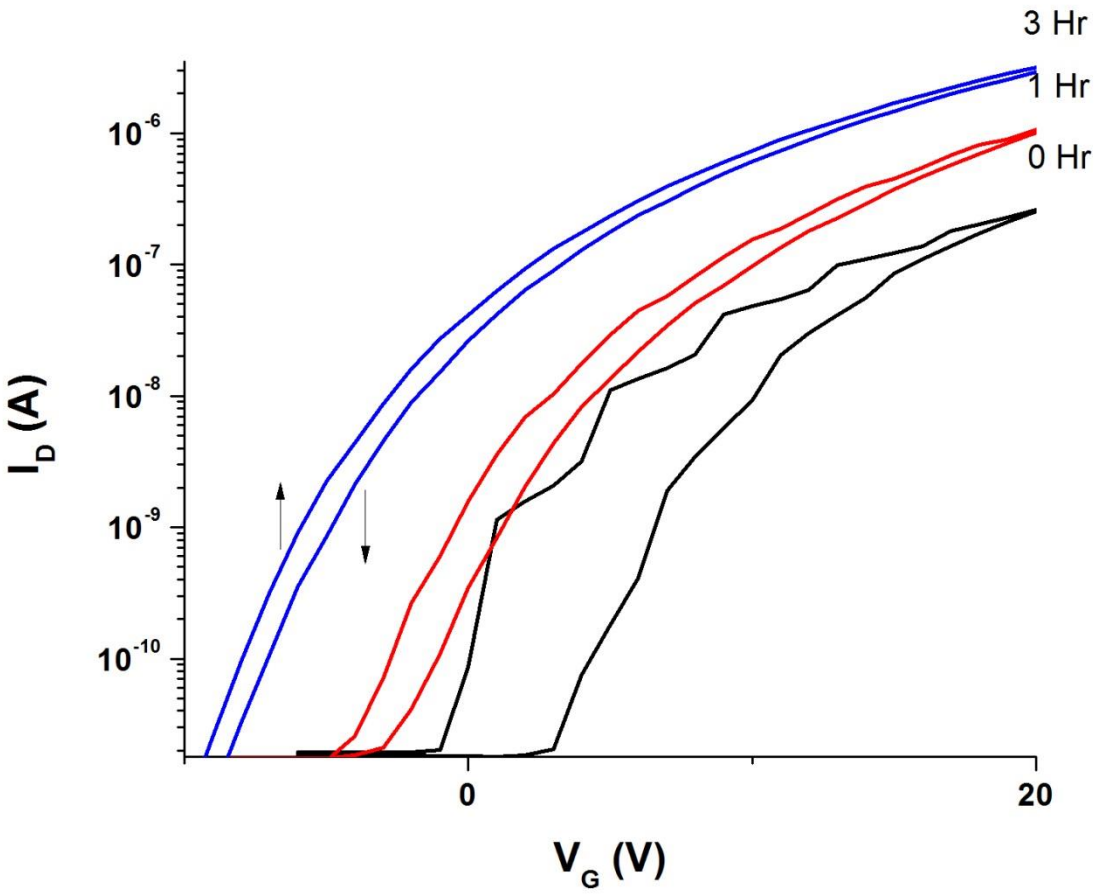

Figure 48 Transfer characteristics of TFTs annealed for different durations revealing hysteresis changes.

5.7 Bottom-Gate TFT on PEN

Four different bottom-gate PEN TFTs were fabricated with GSZO active layers and tested for I-V performance: GSZO TFT with a SiO_2 gate insulator on PEN (TFT-A), TFT with a Si_3N_4 gate insulator (TFT-B), TFTs with Si/su-8/Si_3N_4 (TFT-C) and PEN/su-8/SiO_2 (TFT-D). The devices performance and electrical characteristics are shown in Table 23 and (Figure 49-*Figure 56*). Devices without su-8 yielded lower $I_{ON/OFF}$ ratios of 10^2 and 10^3 with I_D constantly above the current limit needed to establish V_{ON}. Thus for these devices V_{ON} was taken as the voltage at which the I_D begins to increase which is ~-7.5 V and ~-2.5 V for the A and B TFTs. Large SS's above 5 V/dec and smaller μ_{FE} below 0.5 $cm^2/V \cdot s$ were also examined for devices without su-8. Improvement in electrical performance was seen for devices with an su-8 planarization layer (TFTs C and D) which showed $I_{ON/OFF}$ of 10^5, SS ~0.6 V/dec and ~0.7 V/dec and μ_{FE} ~0.5 $cm^2/V \cdot s$ and ~0.7 $cm^2/V \cdot s$. Strong saturation in the output plot of TFT-D can be seen in *Figure 56* however I_D begins to decrease while V_D approaches 20 V. TFT-D was also tested with a decreased time delay (1 s-0.7 s) to examine its effect on the saturation of the output curves (*Figure 57*). It can be seen that saturation of output I_D current does not take place as it had when the same device was tested at a slower rate.

Table 23

Electrical characteristics of plastic GSZO TFT

TFT	TFT	I_{ON} (A)	I_{OFF} (A)	$I_{ON/OFF}$	I_G (A)	SS (V/dec)	V_{ON} (V)	μ_{FE} ($cm^2/V \cdot s$)
TFT-A	SiO_2/PEN	$3.4x10^{-7}$	$8.3x10^{-10}$	10^2	$4.4x10^{-11}$	8.0	-7.5	0.1
TFT-B	Si_3N_4/PEN	$1.8x10^{-8}$	$1.6x10^{-11}$	10^3	$2.9x10^{-12}$	5.4	-2.5	0.06
TFT-C	Su-8/ Si_3N_4/Si	$2.4x10^{-7}$	$1x10^{-12}$	10^5	$2x10^{-11}$	0.6	0.4	0.5
TFT-D	Su-8/ SiO_2/PEN	$3.1x10^{-7}$	$1x10^{-12}$	10^5	$2x10^{-11}$	0.7	0	0.7

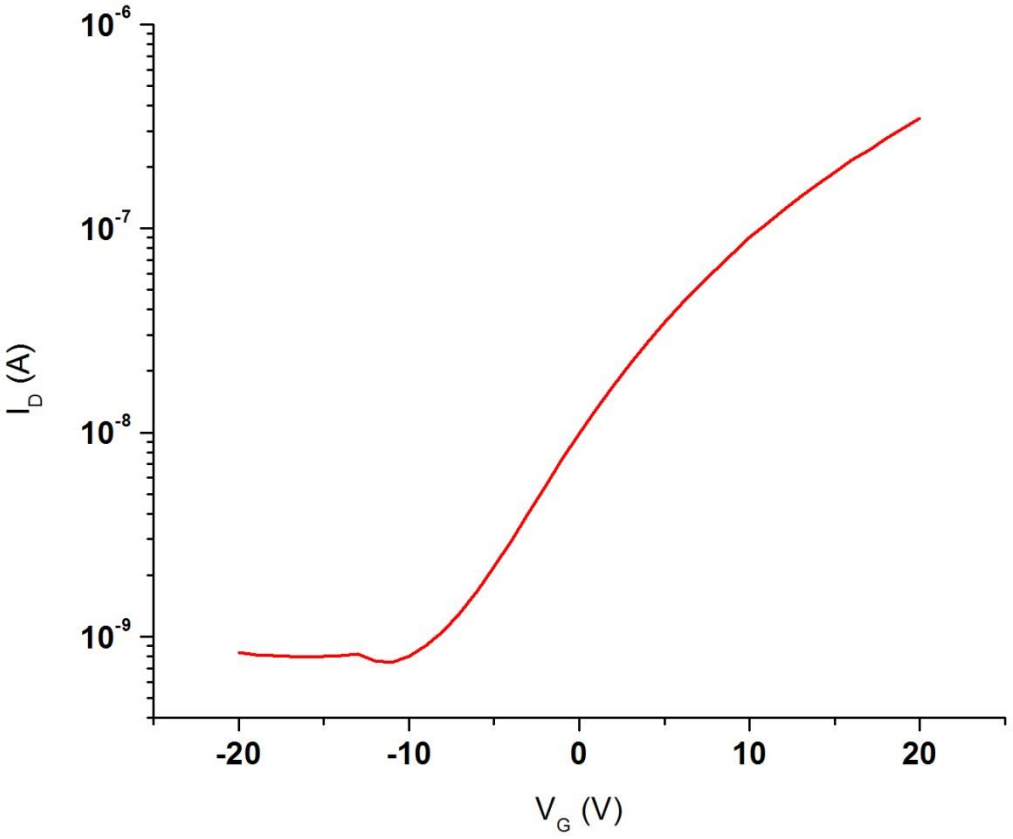

Figure 49 Transfer graph of 15 nm GSZO on PEN with SiO_2.

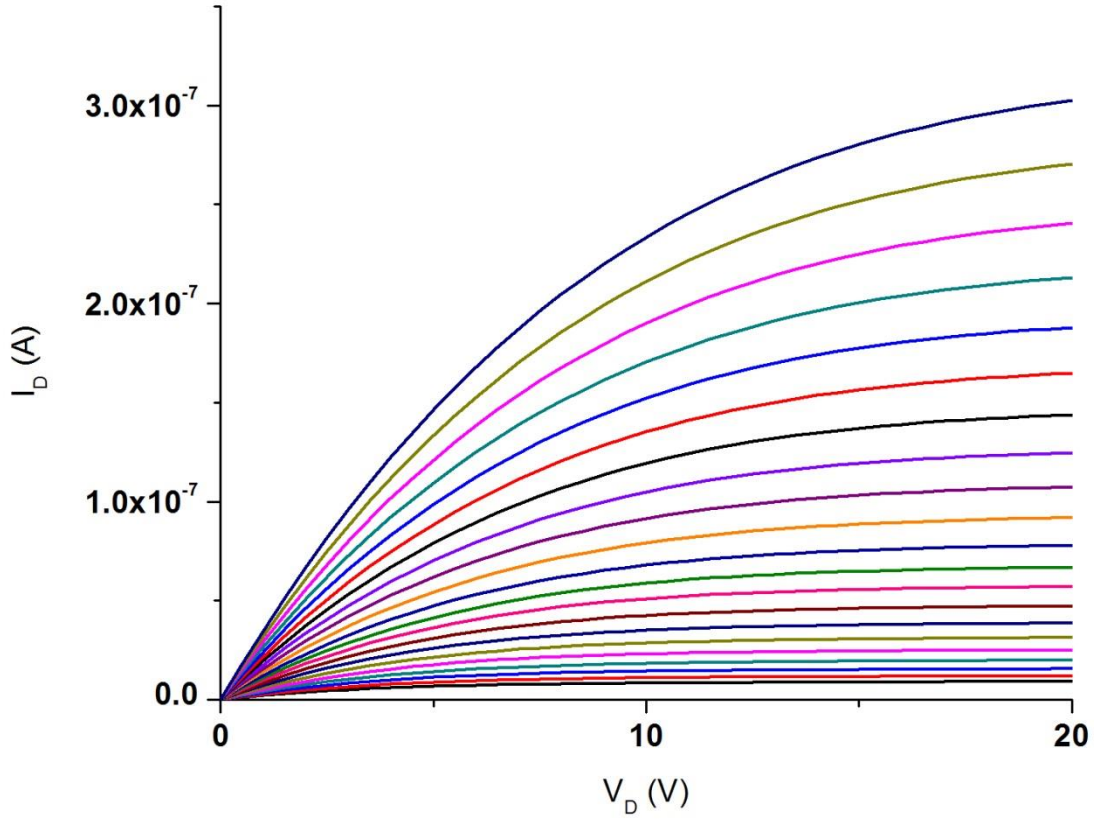

Figure 50 Output graph of GSZO TFT on plastic substrate with SiO_2 gate oxide.

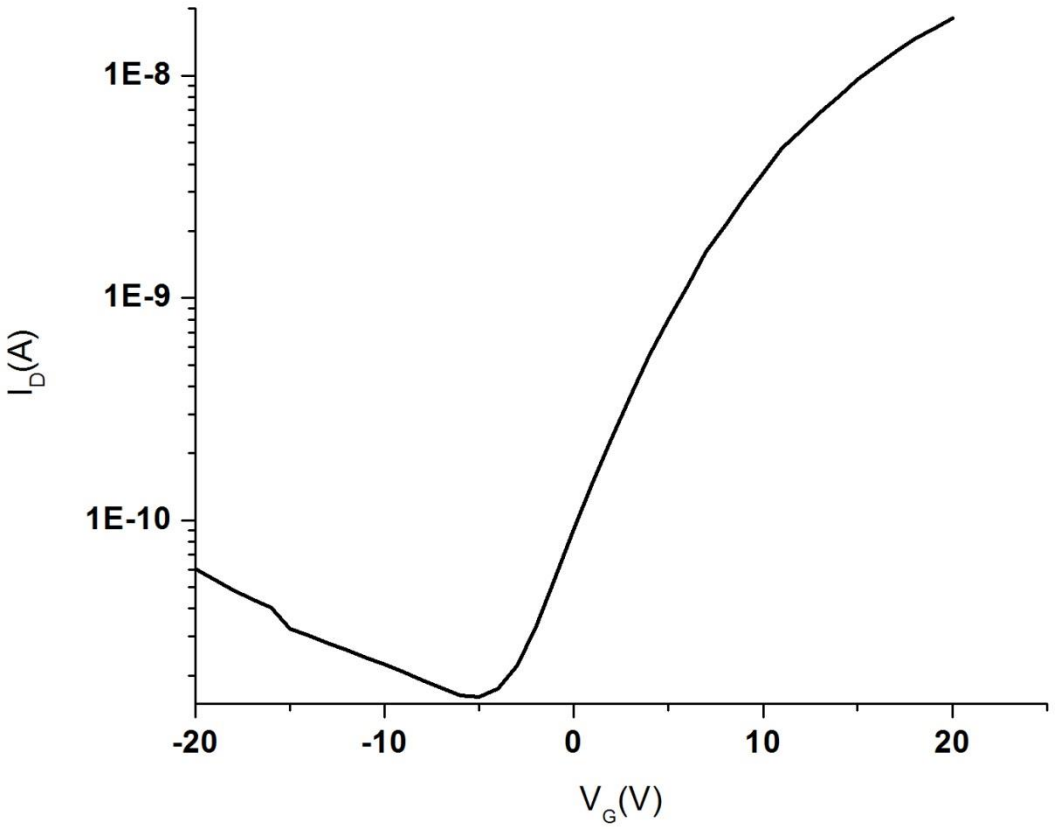

Figure 51 Transfer graph of 15 nm GSZO on PEN with Si_3N_4.

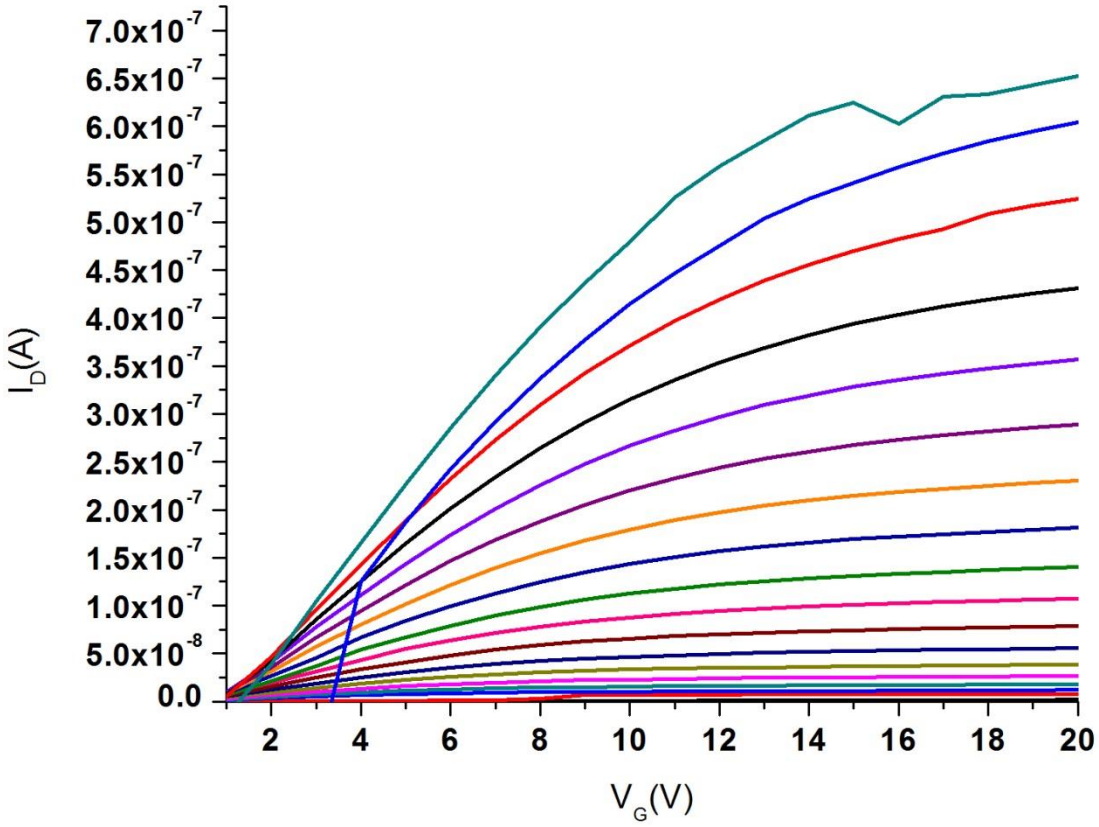

Figure 52 Transfer graph of 15 nm GSZO on PEN with Si_3N_4

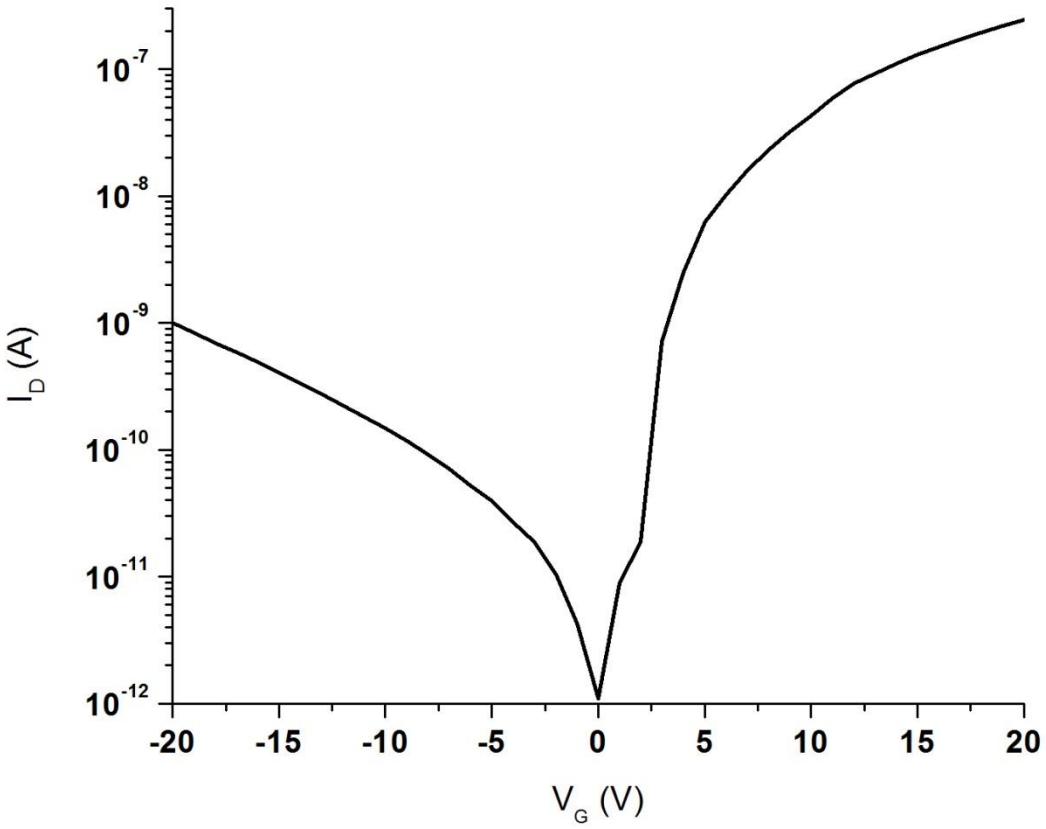

Figure 53 Transfer graph of 15 nm GSZO on Si with 5 mm of Su8.

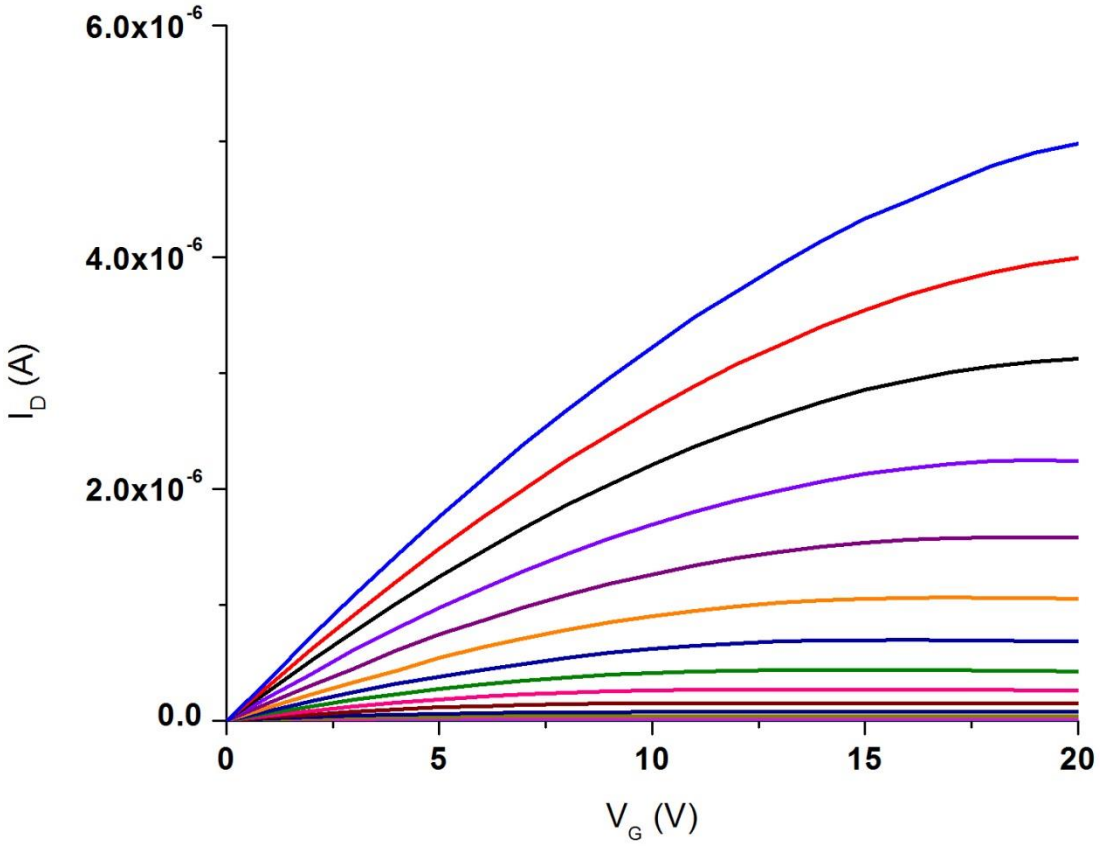

Figure 54 Output graph of 15 nm GSZO on Si with 5 mm of Su8.

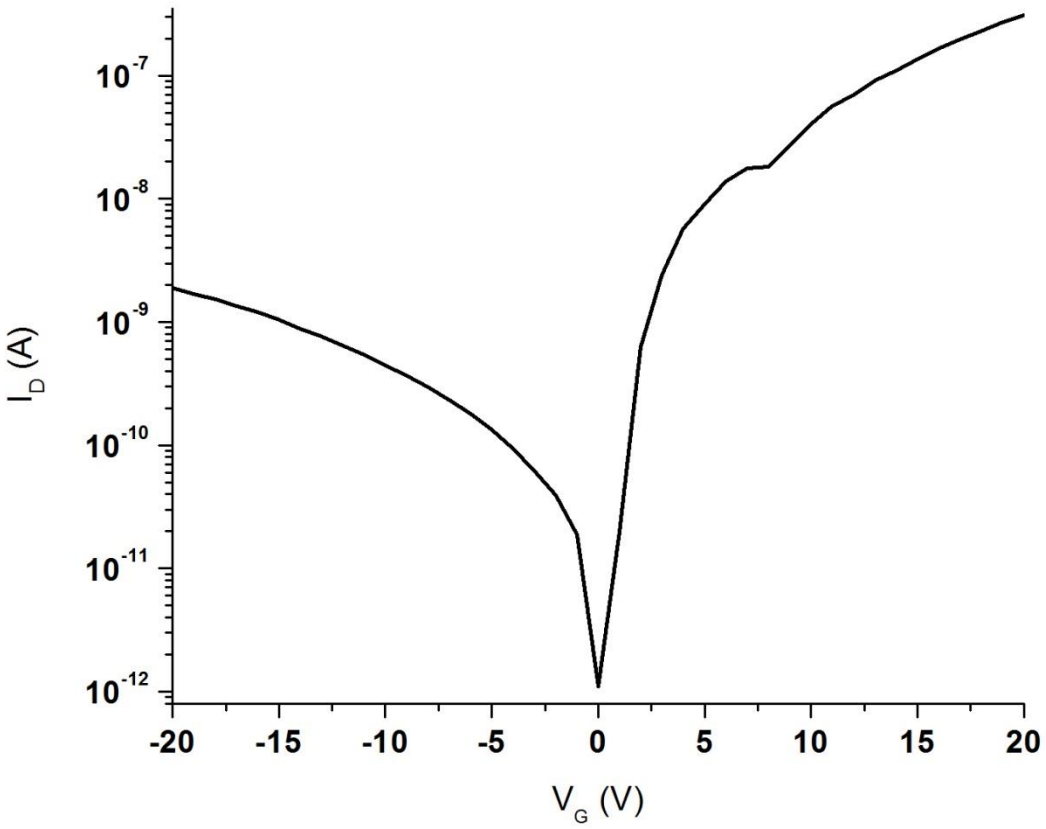

Figure 55 Transfer graph of Su8/SiO_2 GSZO TFT on PEN

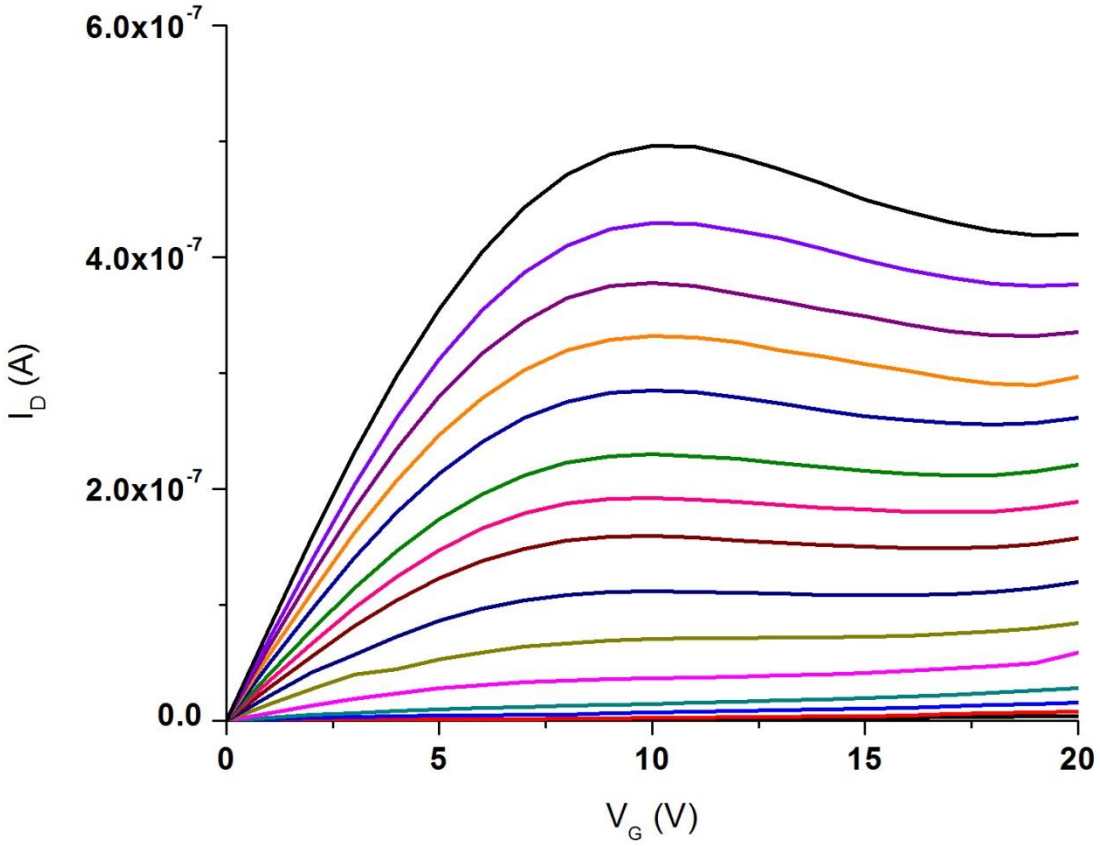

Figure 56 Output graph of Su8/SiO_2 GSZO TFT on PEN measured with normal 1 s delay.

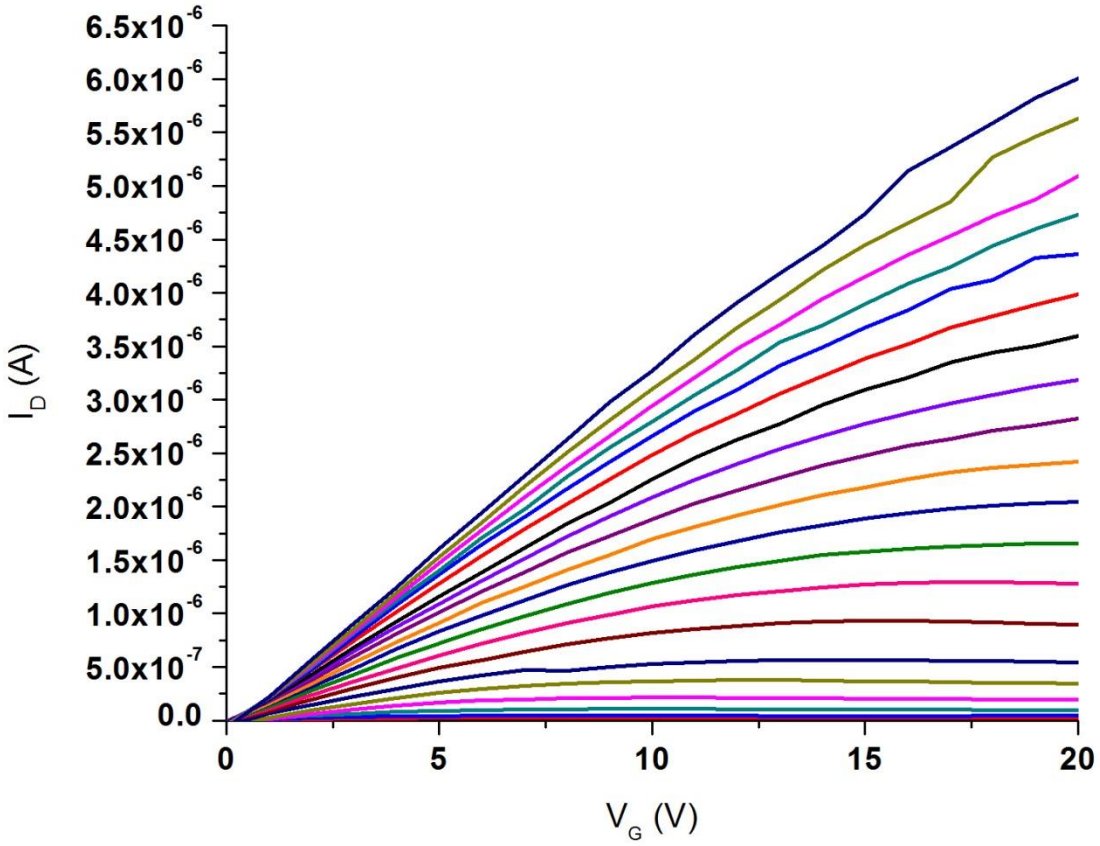

Figure 57 Output graph of Su8/SiO_2 GSZO TFT on PEN measured with faster 0.7 s delay.

5.8 Conclusion

In summary, GSZO-TFTs were fabricated to investigate the effect of deposition parameters on the electrical performance of the TFTs. The device degraded when annealing temperature was reduced however improvements in electrical and compositional properties occurred after increasing annealing duration and the temperature at which the films were deposited. Device hysteresis was shown to reduce with increasing annealing duration and further improvements such as SS and I_{OFF} reduction took place as GSZO film thickness decreased. When compared to films annealed at 450 °C, XPS characterization showed a higher density of Sn^{2+} bonds with more oxygen related defects within the 140 °C film, while the 450 °C annealed device performance was superior. Bottom-gate GSZO TFTs were fabricated on PEN using either Si_3N_4 or SiO_2 as the gate insulator. Devices with planarization su-8 layer were shown to be superior with $I_{ON/OFF}$ of 10^5, SS ~0.6 V/dec and μ_{FE} ~0.7 $cm^2/V \cdot s$.

CHAPTER 6

Deposition Pressure

In this chapter, dependence of GSZO TFT performances as a function of Ar/O_2 pressures during the channel deposition was studied. GSZO TFTs were characterized using I-V and C-V measurements. The electrical and optical stability measurements were also the subject of detailed study. The optical properties of the GSZO thin films deposited under different pressures were studied by absorption measurements while surface and interface morphologies were examined using XRR and AFM measurements. Atomic composition analysis was also conducted by XPS characterizations.

6.1 I-V Characterizations

Table 24 and Figure 58 show the transfer I-V curves of devices with active layers deposited with increasing pressures from 1-10 mTorr. Subsequently all films were annealed at 140 °C for 3 hours in air. With an increase in deposition pressure it is observed that I_{OFF} and I_{ON} decreases, V_{ON} shifts positively and $I_{ON/OFF}$ increases. However the SS (1.12 V/dec) and hysteresis (0.9 V) is lowest for the 5 mTorr device. Hysteresis values were found by calculating the change in V_{ON} (ΔV_{ON} at $I_D=5x10^{-12}$ A) from the forward to reverse I_D sweep. Though the 10 mTorr film has the largest $I_{ON/OFF}$ of $5.2x10^{-6}$ A it also has the largest hysteresis (2 V). D_{IT} is the density of interface traps calculated by the SS (Equation 4) where k-Boltzmann's constant, T-temperature (K), C'-capacitance per unit area of SiO_2 and q-electric charge constant [43].

$$D_{IT} = \left[\left(\frac{Log(e)SS}{kT}\right) - 1\right]\frac{C\prime}{q} \qquad \text{Equation 4}$$

The D_{IT} calculations show the 1 mTorr exhibiting higher interface traps compared to 5 and 10 mTorr devices. Though each device has similar μ_{FE} the 1 mTorr device has the largest

with 0.43 $cm^2/V \cdot s$. The slope of the I-V output curves at V_{GS}=20 V and V_{DS}=15-20 V (Figure 59) was calculated to examine the saturation of the devices. It is shown that the saturation of the devices improves with increasing deposition pressure.

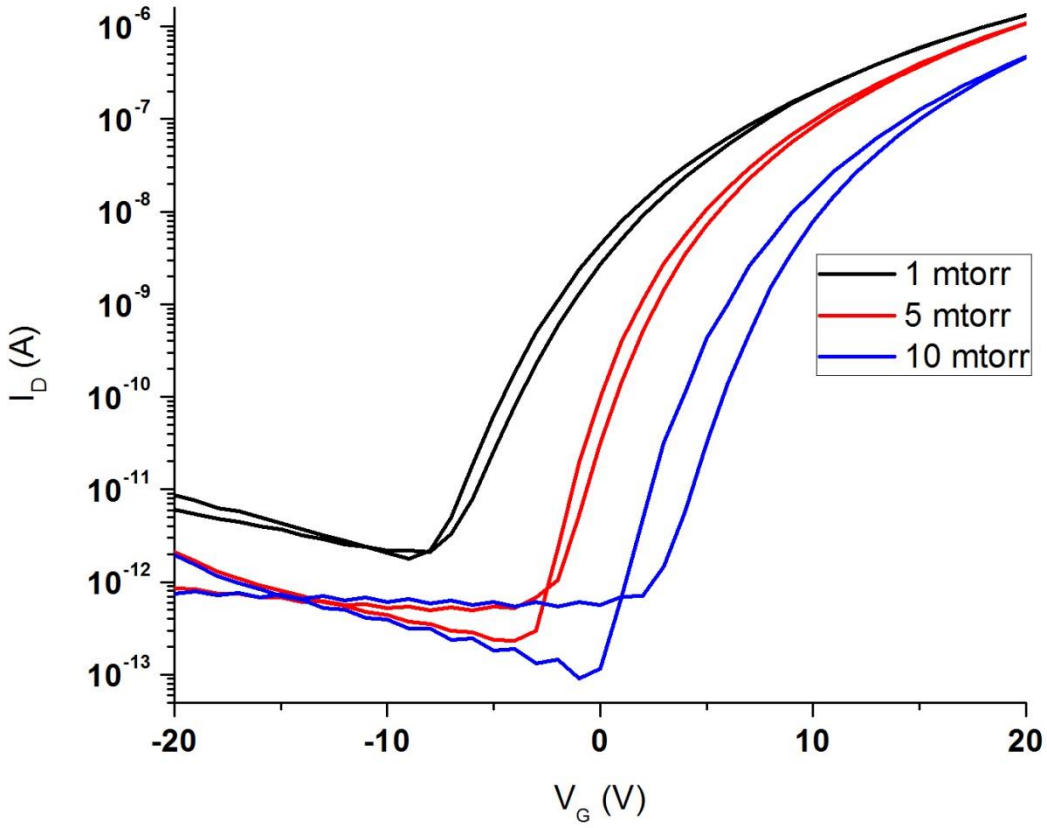

Figure 58 I-V transfer curves of devices with GSZO channel layers deposited at 1, 5 and 10 mTorr.

Table 24

Electrical parameters of GSZO TFTs with channel layers deposited at 1, 5 and 10 mTorr.

	1 mTorr	5 mTorr	10 mTorr
μ_{FE}	0.43	0.2	0.3
SS	1.8	1.1	1.2
V_{ON}	-16	-1.8	2
I_{ON}	$1.3x10^{-6}$	$1.1x10^{-6}$	$4.7x10^{-7}$
I_{OFF}	$1.8x10^{-12}$	$2.3x10^{-13}$	$9.1x10^{-14}$
$I_{ON/OFF}$	$7.4x10^{5}$	$4.7x10^{6}$	$5.2x10^{6}$
ΔV_{ON}	1.3	0.9	2
$D_{IT}(SS)$	$5.4x10^{12}$	$3.2x10^{12}$	$3.5x10^{12}$

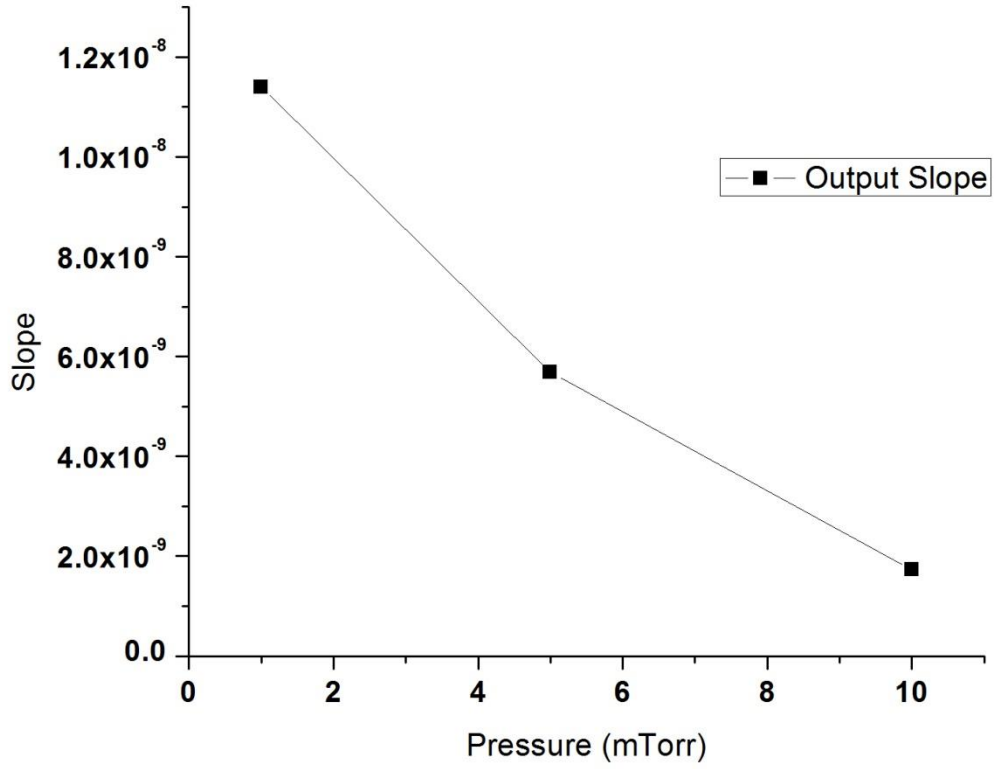

Figure 59 Slope of I-V output curves at V_{GS}= 20 V and V_{DS}=15-20 V.

After 2 months of exposure to air, device degradation for the 1, 5 and 10 mTorr TFTs was analyzed. The transfer graphs of the devices before and after 2 months are shown in Figure 60. It was observed that for all devices, the hysteresis vanished and V_{ON} shifted negatively. The I_{OFF} of the 1 and 10 mTorr devices increased after 2 months while the I_{ON} of the respective devices remained the same. In particular, the 1 mTorr device showed a large increase in I_{OFF}, reducing the $I_{ON/OFF}$ from ~10^6 to ~10^3. In contrast, the 5 mTorr device showed only a slight decrease in both I_{ON} and I_{OFF} resulting in no change in $I_{ON/OFF}$.

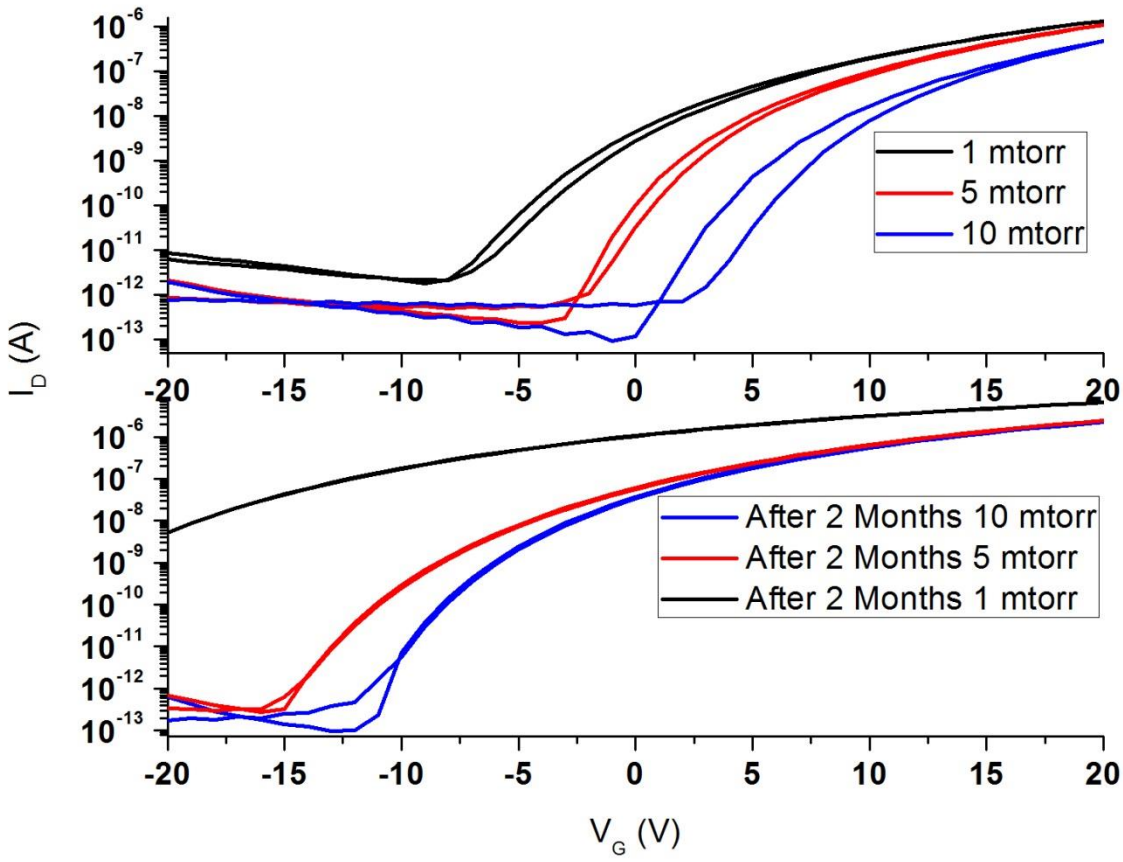

Figure 60 Transfer plots of the 1, 5 and 10 mTorr devices before and after 2 months of exposure to air.

6.2 C-V Characterizations

C-V measurements taken at increasing frequencies (250-1M Hz) are shown in Figure 61-Figure 63. Figure 64 shows the C-V graphs at 250 Hz for all films superimposed. The flat-band voltage (V_{FB}) is the voltage at which the capacitance begins to increase. It can be seen that V_{FB} shifts positively with increasing deposition pressure (-5 V to 2.4 V). It can be seen from Figure 61-Figure 63 that the onset of the accumulation region occurs at smaller V_{GS} voltages and the slope decreases with increasing frequencies. Figure 64 shows the 10 mTorr film has a larger

hysteresis, depletion and accumulation capacitances than all other films. The 5 mTorr film has the smallest hysteresis and the largest slope between the depletion and accumulation regions.

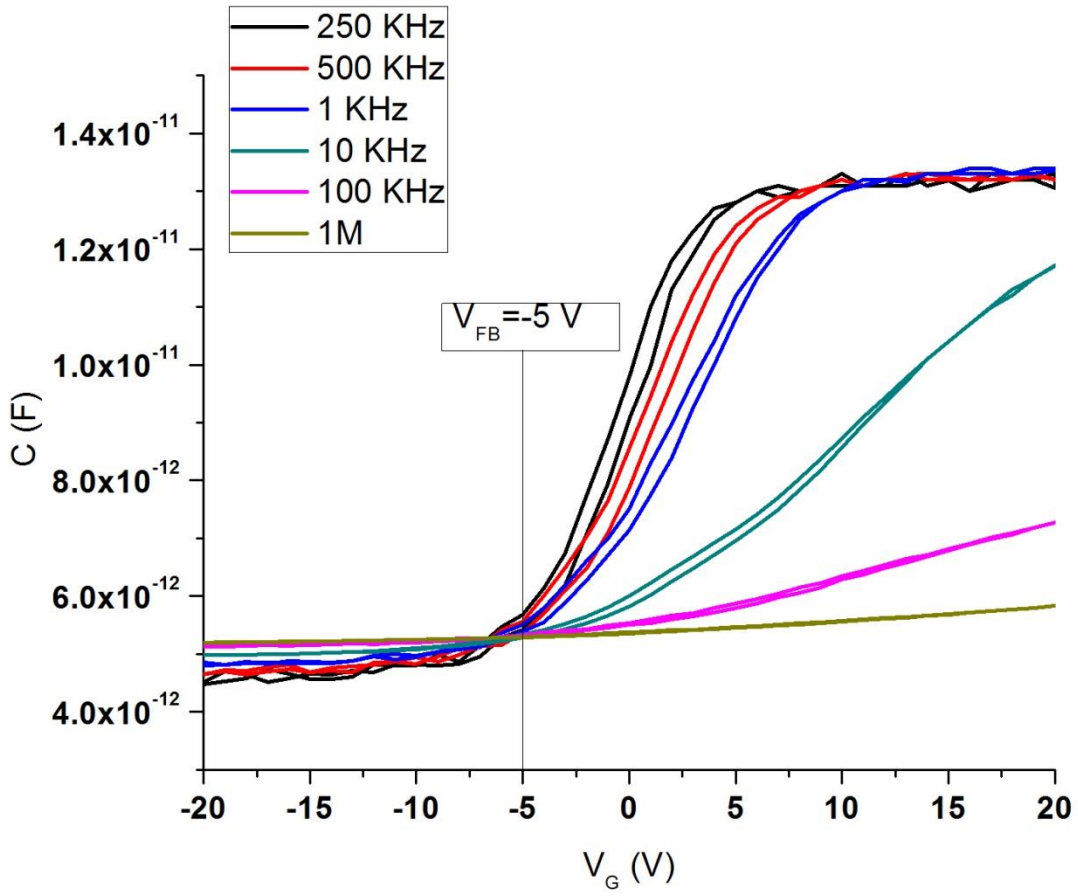

Figure 61 C-V curves of TFT with GSZO layer deposited at 1 mTorr.

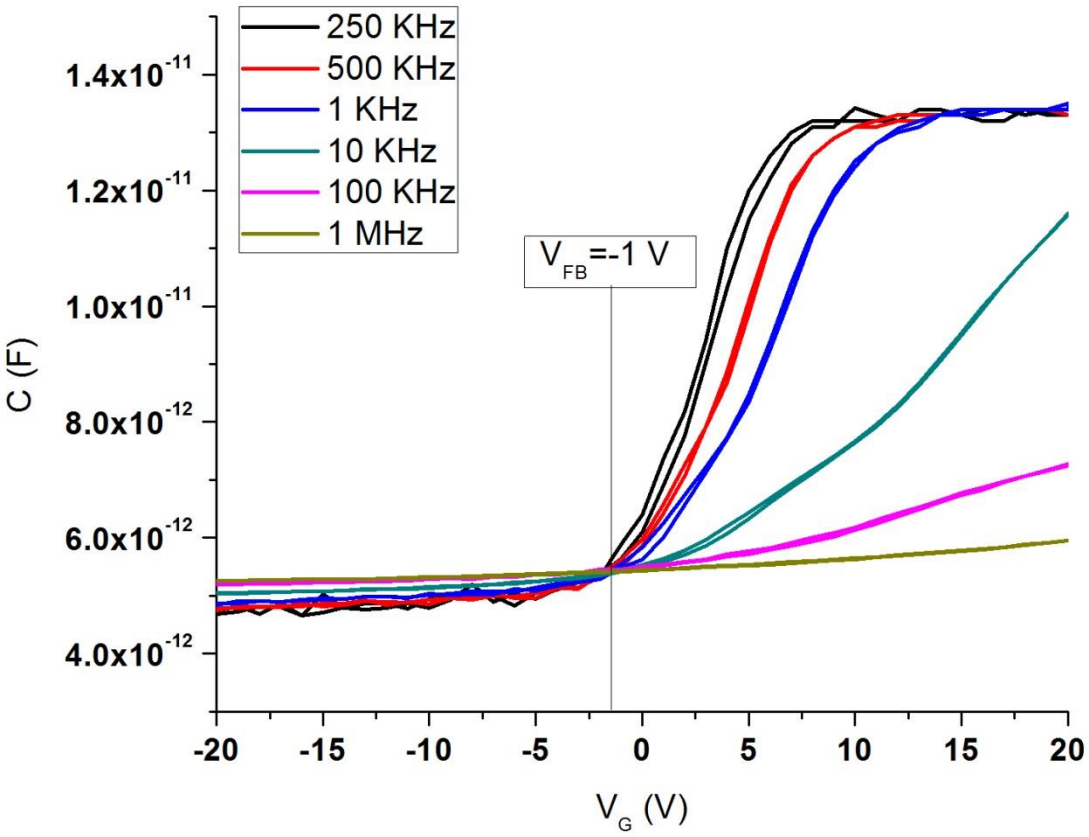

Figure 62 C-V curves of TFT with GSZO layer deposited at 5 mTorr.

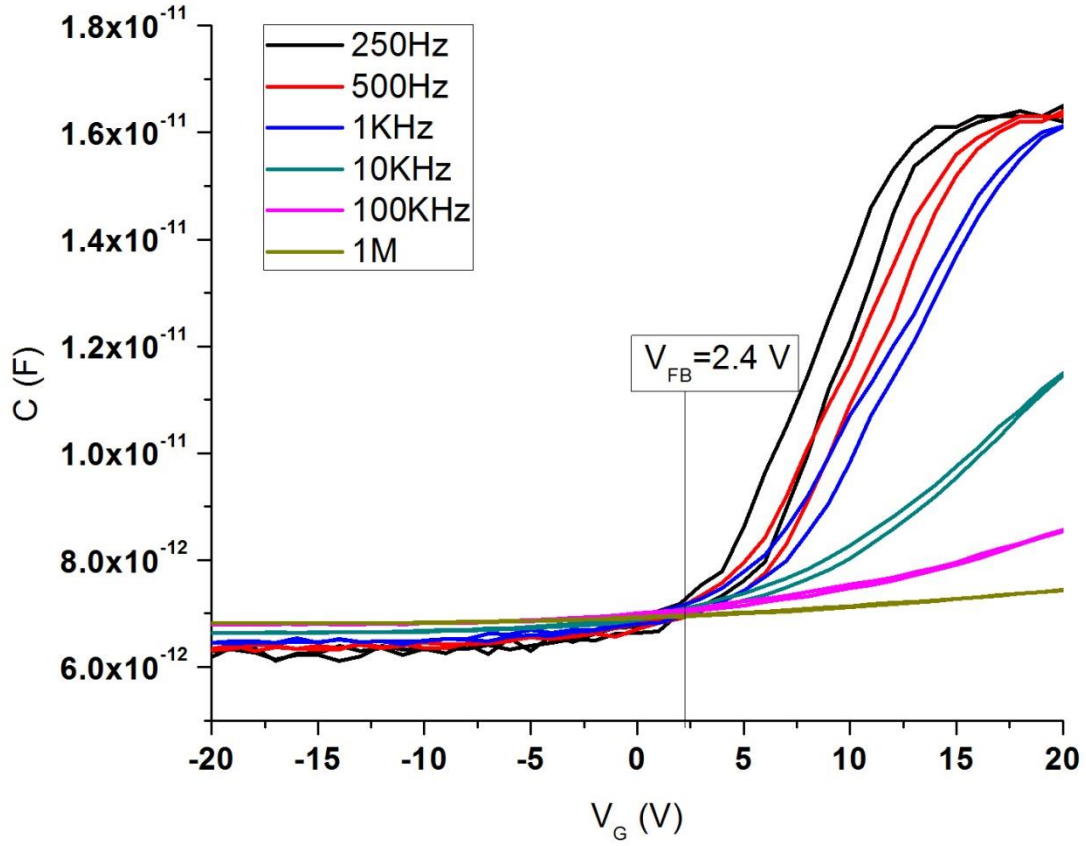

Figure 63 C-V curves of TFT with GSZO layer deposited at 10 mTorr.

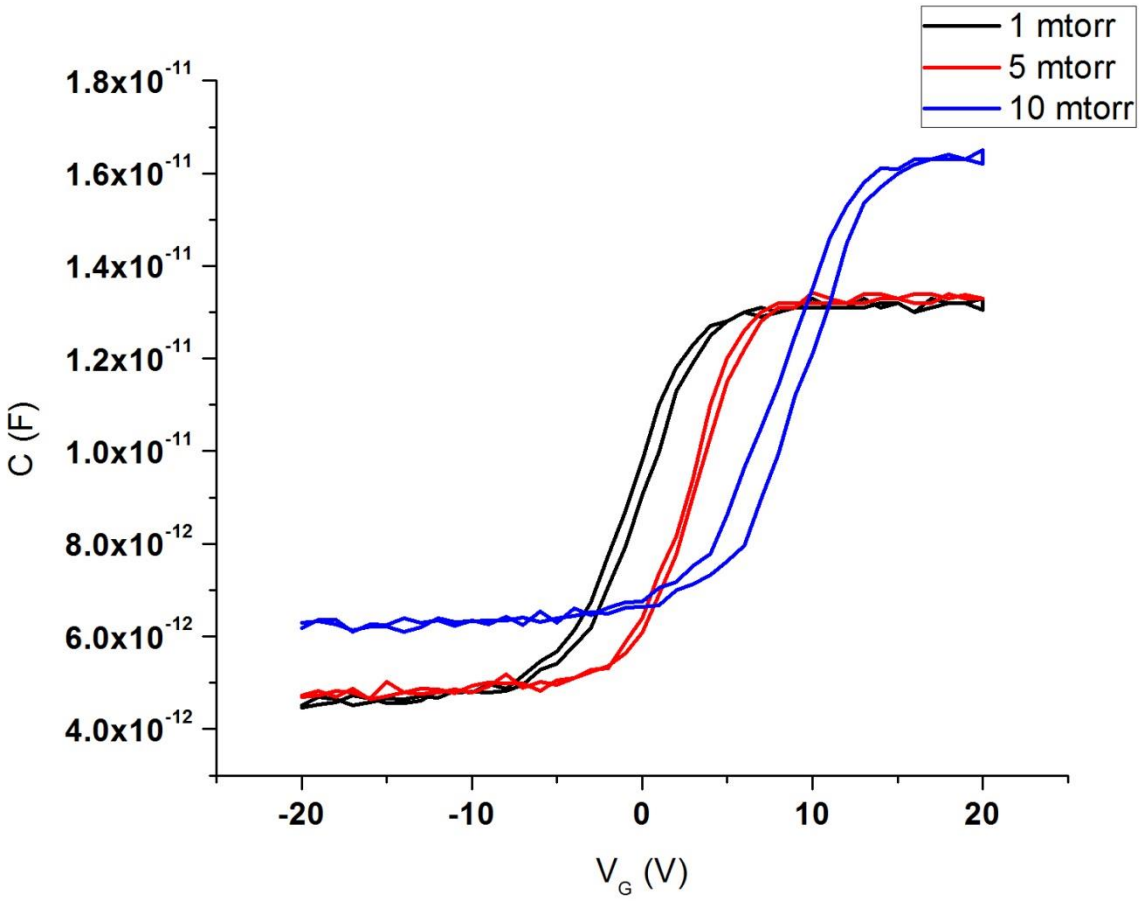

Figure 64 Superposition of C-V curves deposited under different deposition pressures at 250 Hz.

6.3 Morphological Characterizations: XRR & AFM

To examine the effect of deposition pressure on the surface and interface morphologies of the films XRR and AFM measurements were taken to study the film density and roughness. Table 25 shows the values for the density, RMS, skew and kurtosis of the films. The skew is a measure of the height distribution and profile symmetry about the mean line while kurtosis is a measure of the surface sharpness. Figure 65-Figure 67 depicts AFM images (1 μm x1 μm) of the surface of the deposition pressure dependent films. It is found that the density of the films increase and the surface root-mean-square roughness (R_{rms}) decreases with deposition pressure. The largest density (7 kg/cm) and smallest R_{rms} (19.7 pm) can be found in the 10 mTorr film.

The 1 mTorr film is the only film with both a positive skew and a negative kurtosis, while the other two films exhibited opposite.

Table 25

Film density and surface roughness of films deposited at different pressures as determined from XRR and AFM characterizations.

Deposition Pressure	Density (kg/cm^3)	R_{rms} (pm)	Skew	Kurtosis
1 mTorr	5.4	35.4	0.068	-0.0354
5 mTorr	6	27.9	-0.917	2.96
10 mTorr	7	19.7	-0.278	1.14

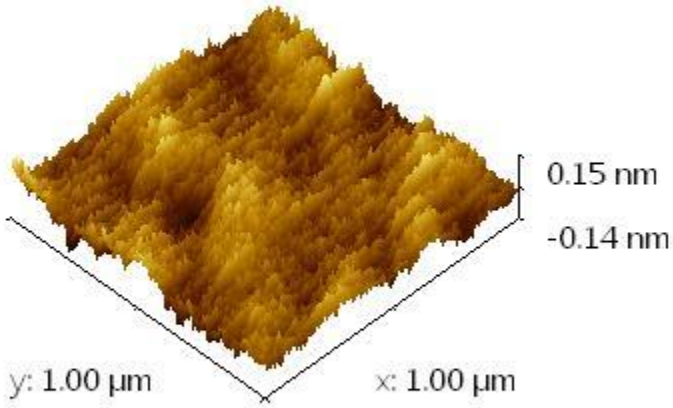

Figure 65 AFM images of a-GSZO films deposited at 1 mTorr deposition pressure

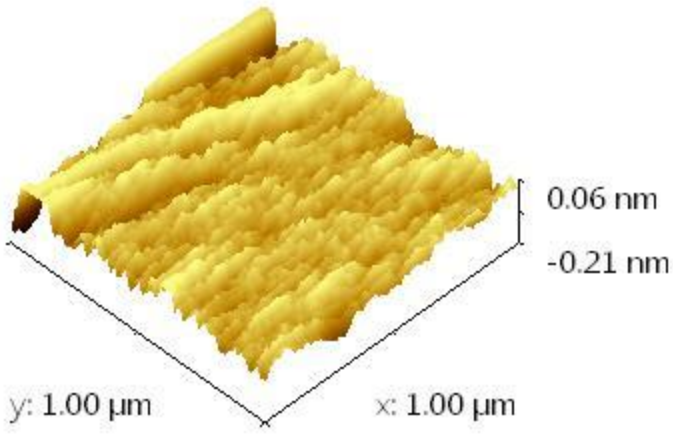

Figure 66 AFM images of a-GSZO films deposited at 5 mTorr deposition pressure

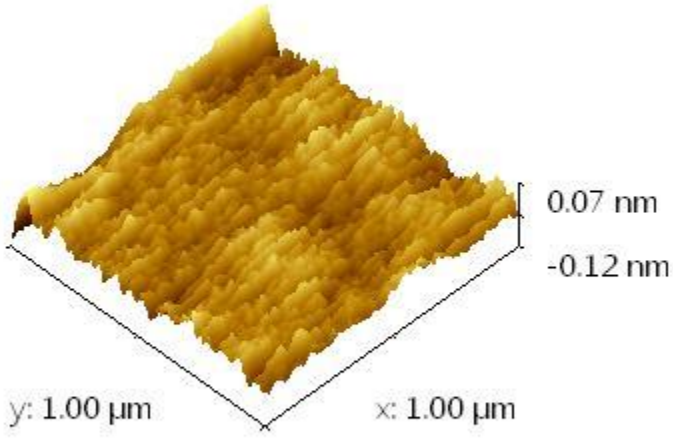

Figure 67 AFM images of a-GSZO films deposited at 10 mTorr deposition pressure

6.4 Atomic Composition Analysis: XPS

XPS characterization was done on the surface and 5 nm below 15 nm GSZO films deposited at 1, 5 and 10 mTorr pressures to examine the effect of annealing temperature on atomic composition (Table 26). It can be seen deposition pressure has little effect on the atomic composition of the films at both the surface and the bulk. Table 27 and Figure Figure *68*-Figure 70 show the O 1s spectra de-convoluted into three peaks of different states, i.e., 530.2 eV (OI), 531.7 eV (OII) and 532.7 eV (OIII). Though the surface of all films have similar at.% ratios the 5 mTorr film shows an increase in OI and decrease in OII at.%. Table 28 and Figure 71-Figure 73 show the Sn relative at.% as a function of annealing temperature. The Sn^{2+} relative at.% within the bulk of the films decrease (84.4 to 23 at.%) causing a dramatic increase in Sn^{4+} relative at.% (15.6 to 77 at.%) with film deposition pressure increase from 1 to 10 mTorr.

To analyze the presence of Zn_I within the GSZO films the Auger $ZnL_3M_{4.5}M_{4.5}$ spectra were investigated with the two Auger peaks at 498 and 494.5 eV attributed to the Zn-O bonds and the Zn_I , respectively [44]. *Figure 74* shows the percentage of Zn_I to Zn-O bonds within the top 5 nm of the GSZO films as a function of pressure which clearly show a decrease in Zn_I with increasing deposition pressure.

Table 26

Atomic percentage of 15 nm GSZO films deposited at 1, 5 and 10 mTorr pressures.

Deposition Pressure	O-(Zn,Ga,Sn)	Cl	Zn	Ga	Sn
1 mTorr Surface	53.3	0.9	40.5	2.8	2.5
1 mTorr Sputtered	44.3	0.1	50.3	4.1	1.2
5 mTorr Surface	53.6	1.0	41.1	2.2	2.2
5 mTorr Sputtered	47.7	0.1	46.6	4.6	1.0
10 mTorr Surface	53.4	1.0	41.0	2.3	2.3
10 mTorr Sputtered	43.8	0.0	50.4	4.4	1.4

Table 27

O-1s related relative percentage of 15 nm GSZO films deposited at 1, 5 and 10 mTorr pressures.

Deposition Pressure	O Relative %			Binding Energy (eV)		
	OI	OII	OIII	OI	OII	OIII
1 mTorr Surface	60	35	6	530.3	531.8	532.8
1 mTorr Sputtered	83	17	1	530.3	531.7	532.7
5 mTorr Surface	61	34	5	530.2	531.7	532.7
5 mTorr Sputtered	76	24	0	530.3	531.7	532.7
10 mTorr Surface	59	34	6	530.3	531.7	532.6
10 mTorr Sputtered	83	17	0	530.2	531.7	532.7

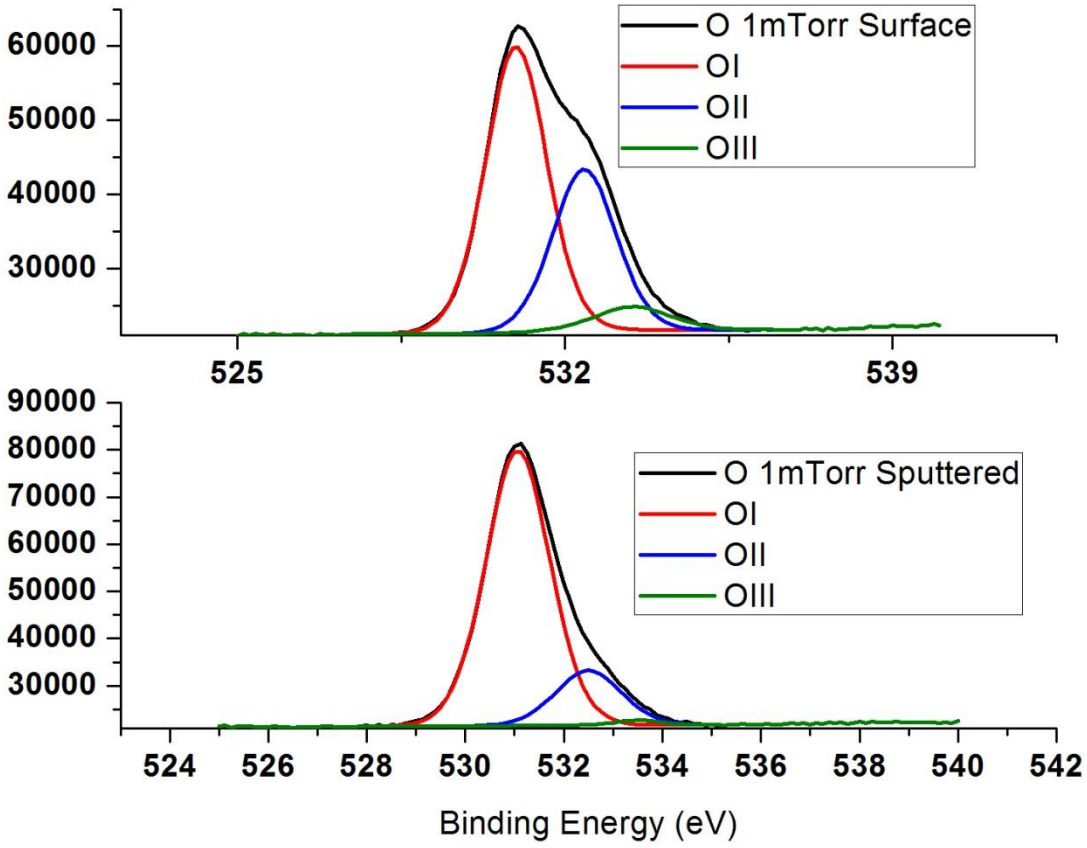

Figure 68 XPS spectra of O ions in GSZO films deposited at 1 mTorr.

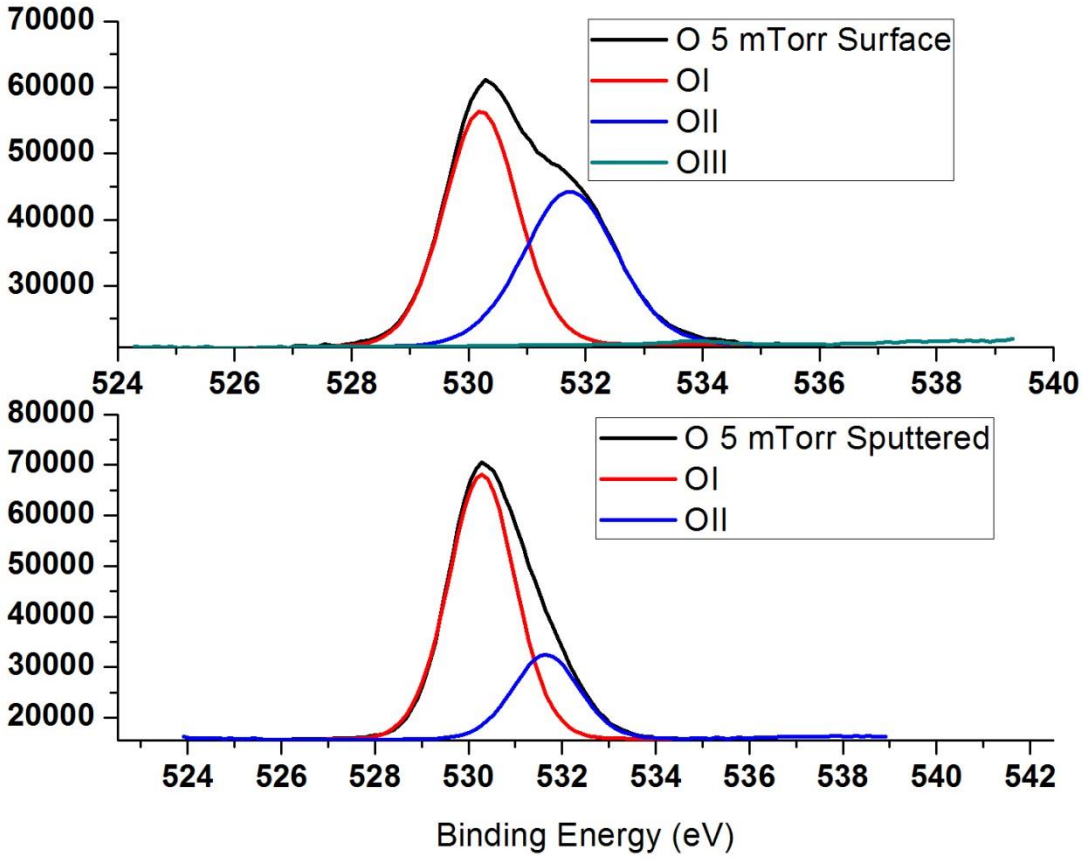

Figure 69 XPS spectra of O ions in GSZO films deposited at 5 mTorr.

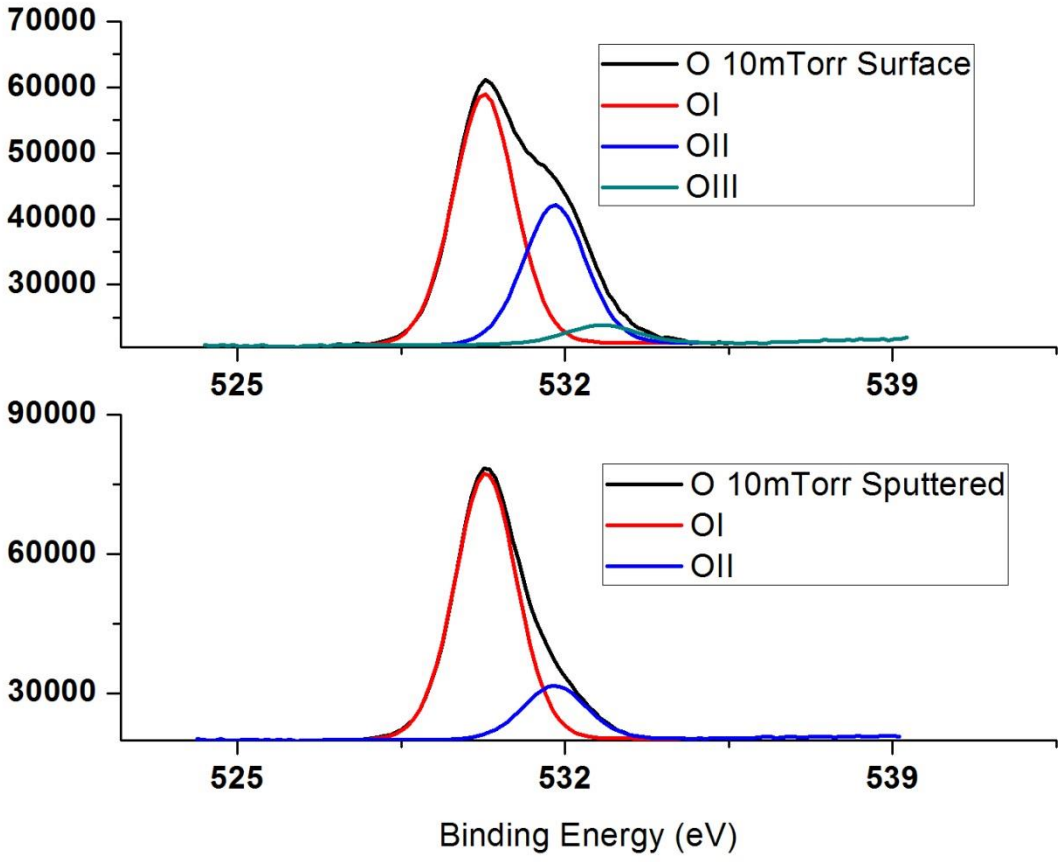

Figure 70 XPS spectra of O ions in GSZO films deposited at 10 mTorr.

Table 28

Sn related relative percentage of 15 nm GSZO films deposited at 1, 5 and 10 mTorr.

Deposition Pressure	Sn Relative%			Binding Energy (eV)		
	Sn^{2+}	Sn^{4+}	Sn^{0}	Sn^{2+}	Sn^{4+}	Sn0
1 mTorr Surface	25.2	74.8	0	486.2	486.8	0
1 mTorr Sputtered	84.4	15.6	0	486.3	487.1	0
5 mTorr Surface	14.1	85.9	0	486.2	486.8	0
\ 5 mTorr Sputtered	74.6	25.4	11.9	486.3	487.1	484.5
10 mTorr Surface	26.2	73.8	0	486.2	486.8	0
10 mTorr Sputtered	23	77	0	486.4	486.8	0

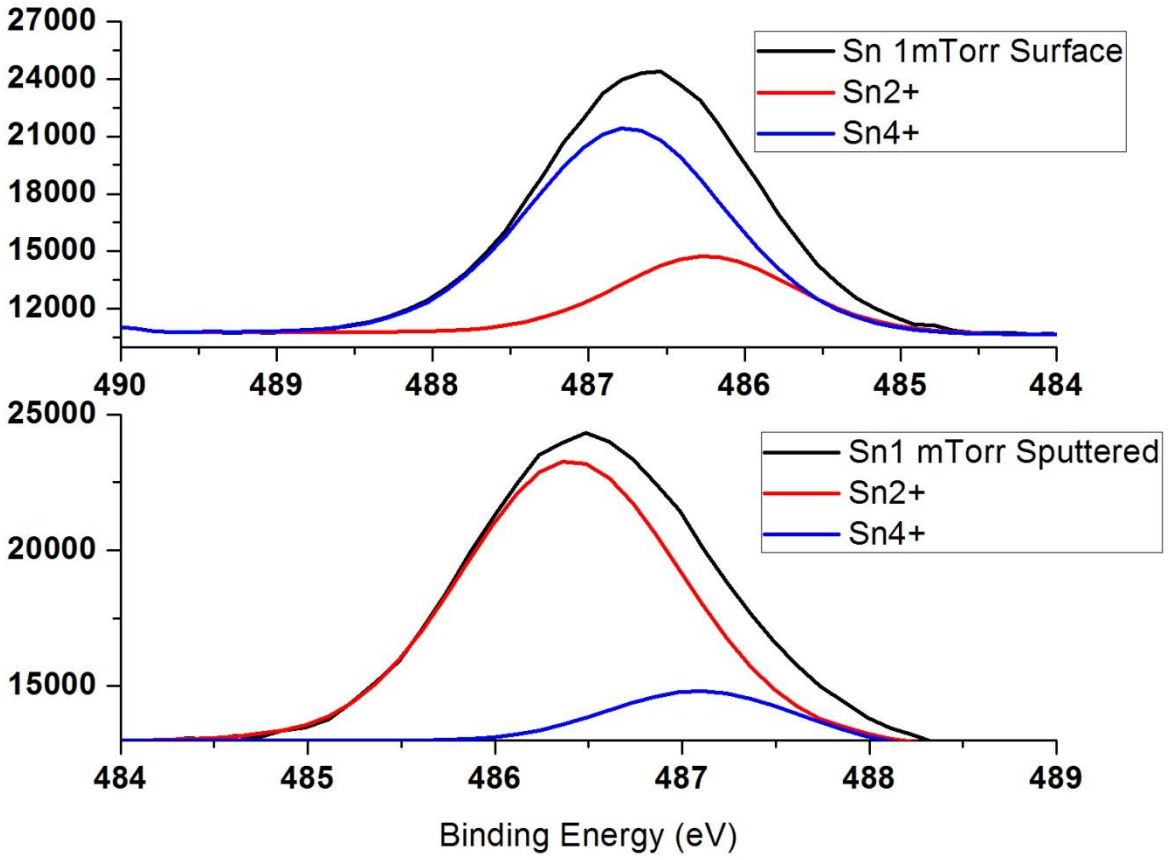

Figure 71 XPS spectra of Sn ions in GSZO films deposited at 1 mTorr.

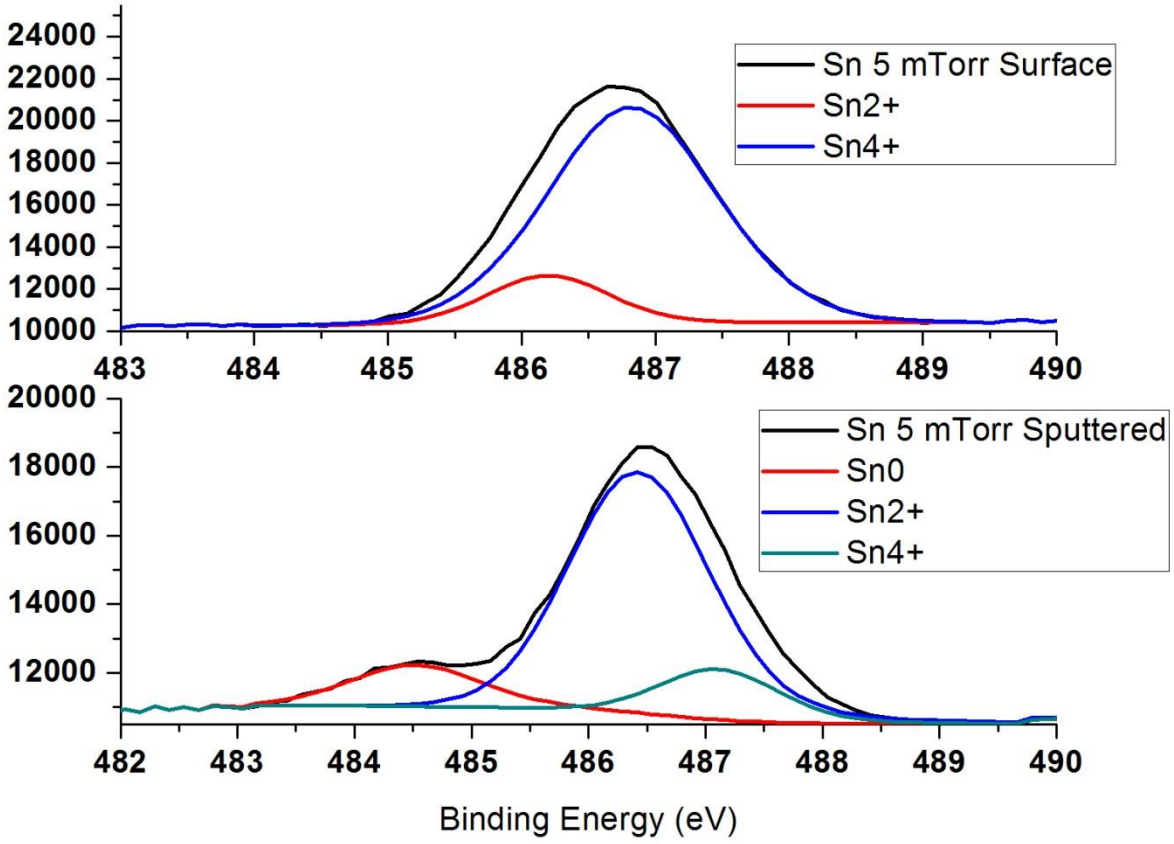

Figure 72 XPS spectra of Sn ions in GSZO films deposited at 5 mTorr.

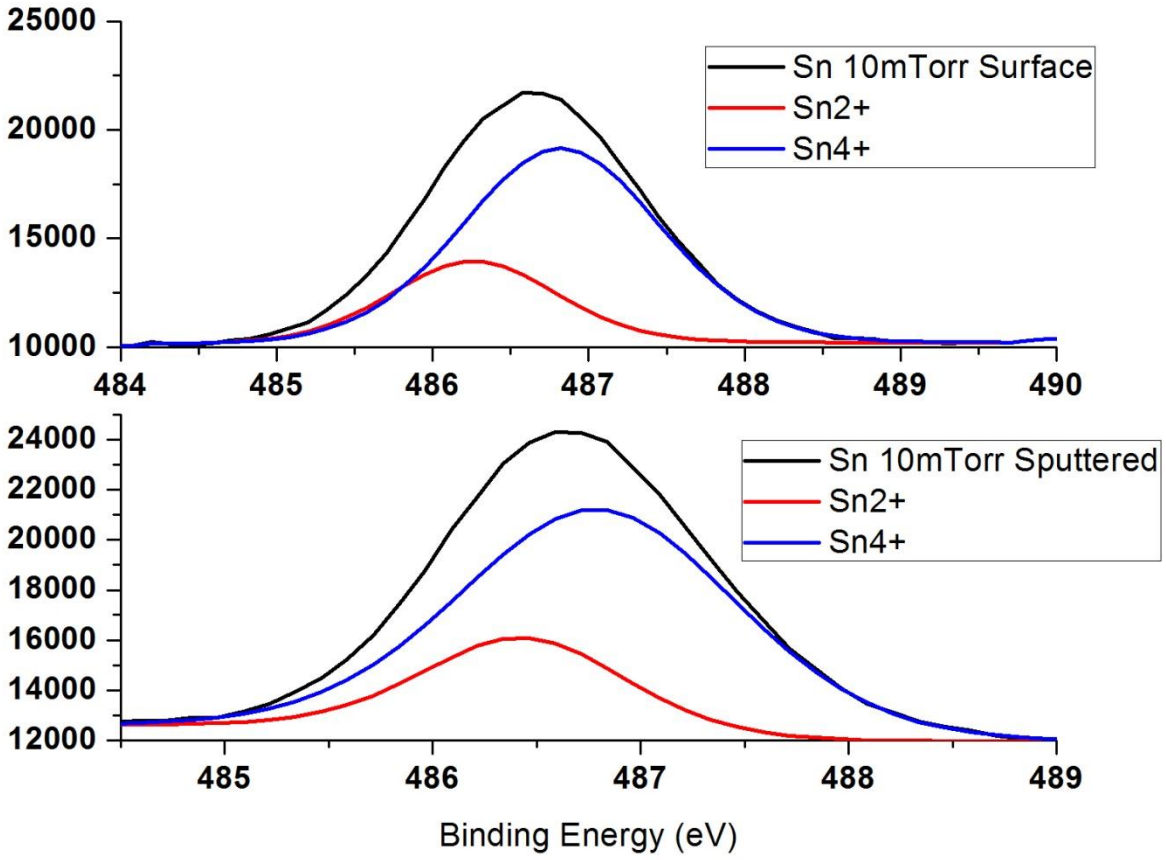

Figure 73 XPS spectra of Sn ions in GSZO films deposited at 10 mTorr.

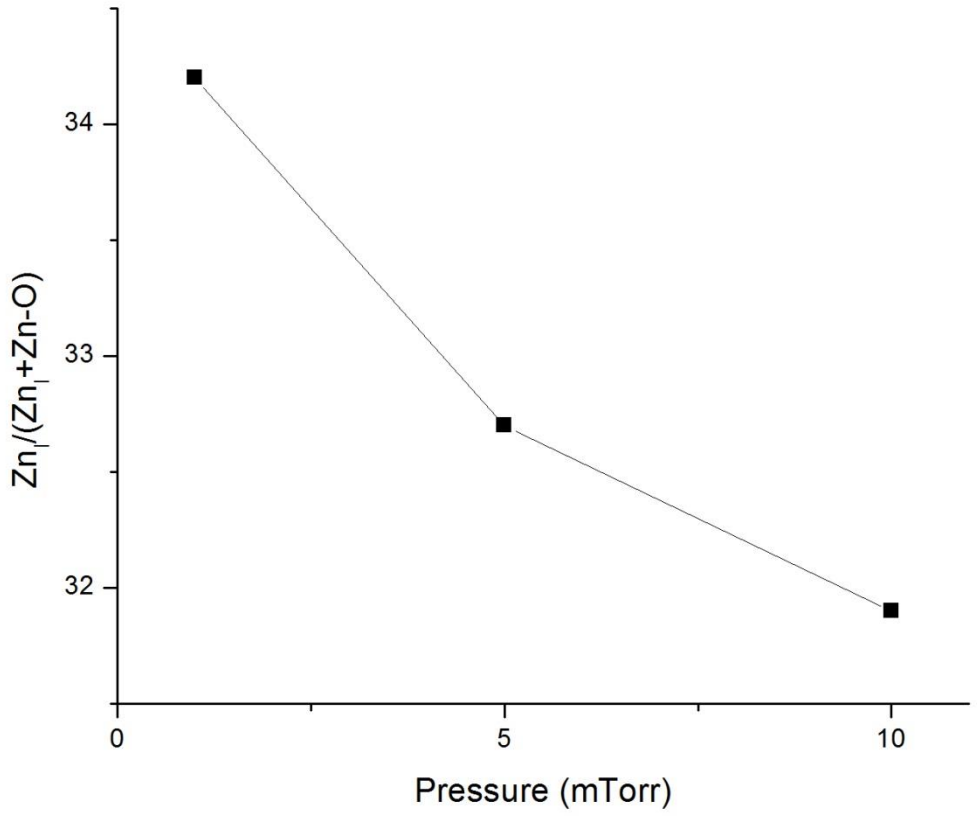

Figure 74 Percentage of Zn_I in first 5 nm of GSZO film as a function of pressure.

6.5 Optical Characterization: Absorption Measurements

To study the optical properties of the a-GSZO films as a function of pressure transmission measurements were taken to examine the transparency of the films as well as find the absorption coefficient as a function of photon energy also known as the Tauc plot. The optical gap of the a-GSZO films can be extrapolated by projected the x-intercept of the slope of the absorption coefficient curves. The Tauc plot in Figure 75 shows the optical gap of the a-GSZO films to be between 3.5-3.51 eV when deposited in pressures between 1 mTorr and 10 mTorr with the latter film exhibiting slightly higher absorption edge. The transmission plot in

Figure 76 shows the amount of incident light that passed through the films for wavelengths between 200 nm and 800 nm.

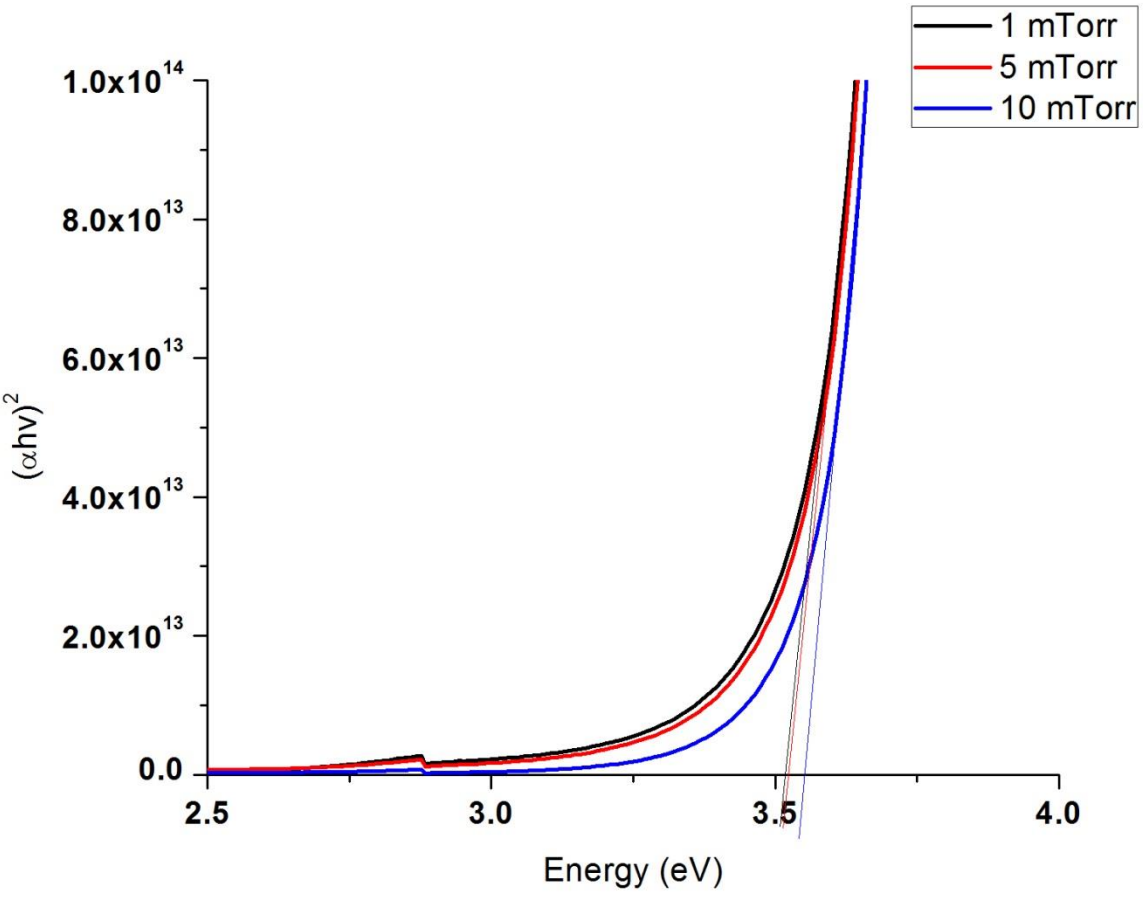

Figure 75 Optical absorption spectra of a-GSZO films deposited in chamber pressures of 1, 5 and 10 mTorr.

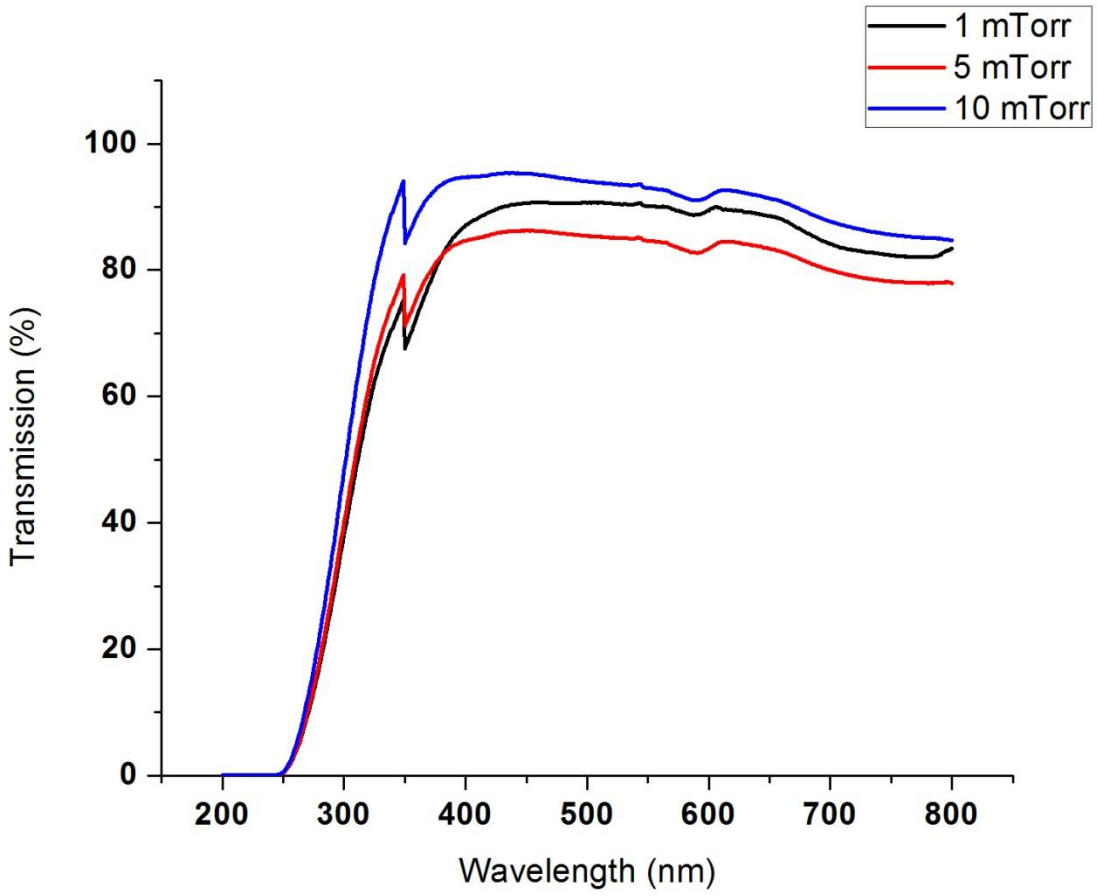

Figure 76 Transmission plot of pressure dependent films

6.6 Photo and Electrical-stability Characterization

Figure 77-Figure 79 show the typical transfer curves of the a-GSZO TFT under illumination stress at three different wavelengths (λ) of 650 nm, 550 nm and 410 nm for 2 hours. An increase in V_{ON} is seen for all devices optically stressed with 650 nm wavelength light only initially after 10 minutes and remains stable thereafter, while I_{OFF} and SS remain invariant. With 550 nm illumination all devices show again initially only a slight positive shift in ΔV_{ON} followed by a negative shift in ΔV_{ON} for 1 hr illumination and t remains stable thereafter. While the 1 mTorr shifts near to its initial V_{ON} state, 5 and 10 mTorr devices shift further negative and show an increase in $I_{ON/OFF}$ after 10 minutes. Further decreasing the wavelength of the light to 410 nm

showed a much larger negative shift in ΔV_{ON} while I_{ON} and I_{OFF} increased for all devices even after 10 minutes stress. Only slight changes in SS can be seen for the 650 nm and 550 nm photo-stressed devices however the 410 nm stressed devices show noticeable degradations in SS even after 2 hours. Negative bias stress (NBIS) tests were conducted on the pressure-dependent devices to examine how stable the devices are with a negative bias applied to the gate with a 550 nm light shone on the active layer. The transfer graphs are shown in Figure 80. It can be seen that after 10 minutes the 1 mTorr device showed a positive shift in ΔV_{ON} while no change can be seen for the 5 mTorr device and a negative shift for the 10 mTorr device. A further negative shift can be seen for all devices with the 10 mTorr device exhibiting the largest shift of ΔV_{ON}= -17.5 V. The I_{OFF} and SS remain invariant for all devices. *Figure 81* shows the change in carrier concentration (ΔN_e), as calculated from Equation 5 with C_i-capacitance per unit area, ΔV_{ON}-change in V_{ON}, q-electric charge and t_{CH}-channel thickness, within the GSZO films as a function of light wavelength as well as associated density of traps.

$$\Delta N_e = \frac{C_i \Delta V_{ON}}{q t_{CH}} \qquad \text{Equation 5}$$

It can be seen that the carrier concentration within the film decreases after 650 nm stress for all devices yet increases for 550 nm and 410 nm stresses. The 10 mTorr showed the largest positive ΔN_e for 550 nm stress while the 5 mTorr device showed the largest positive ΔN_e for 410 nm stress.

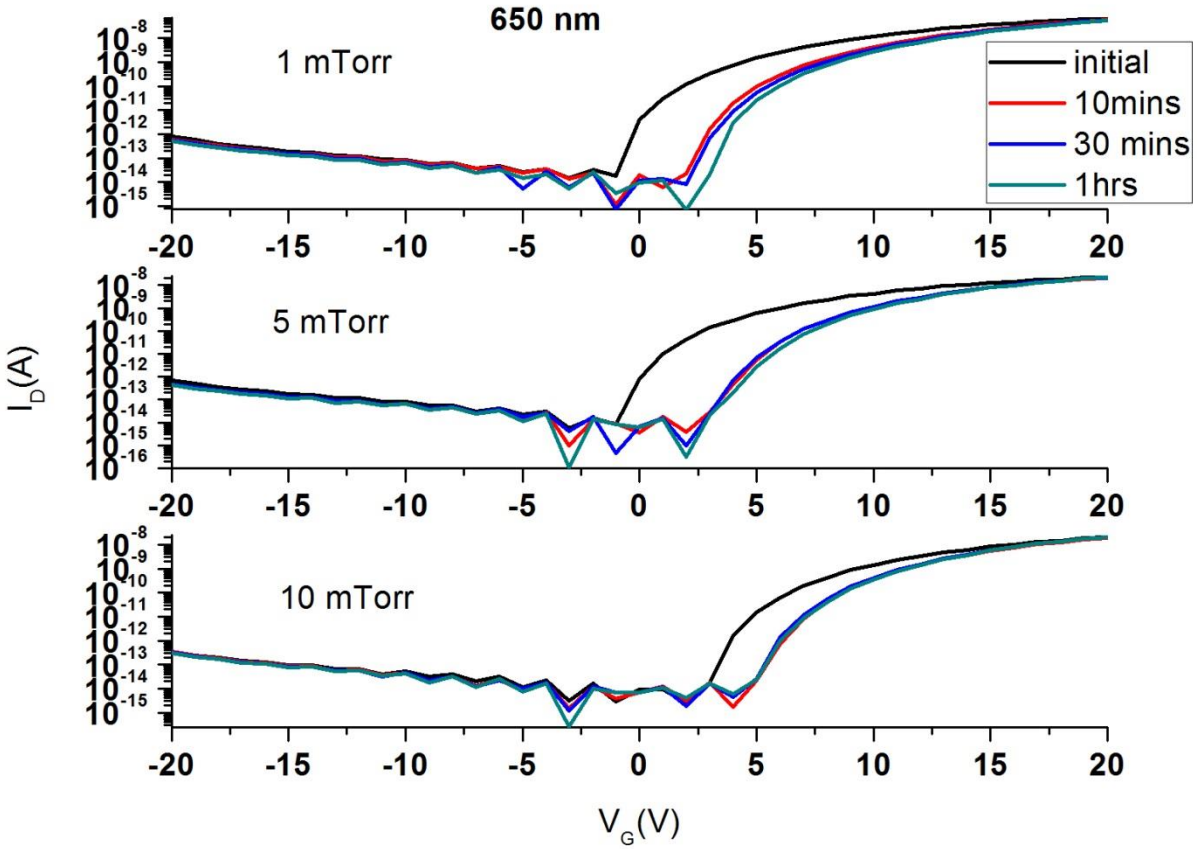

Figure 77 I-V transfer plots of 650 nm photo stability results as a function of duration.

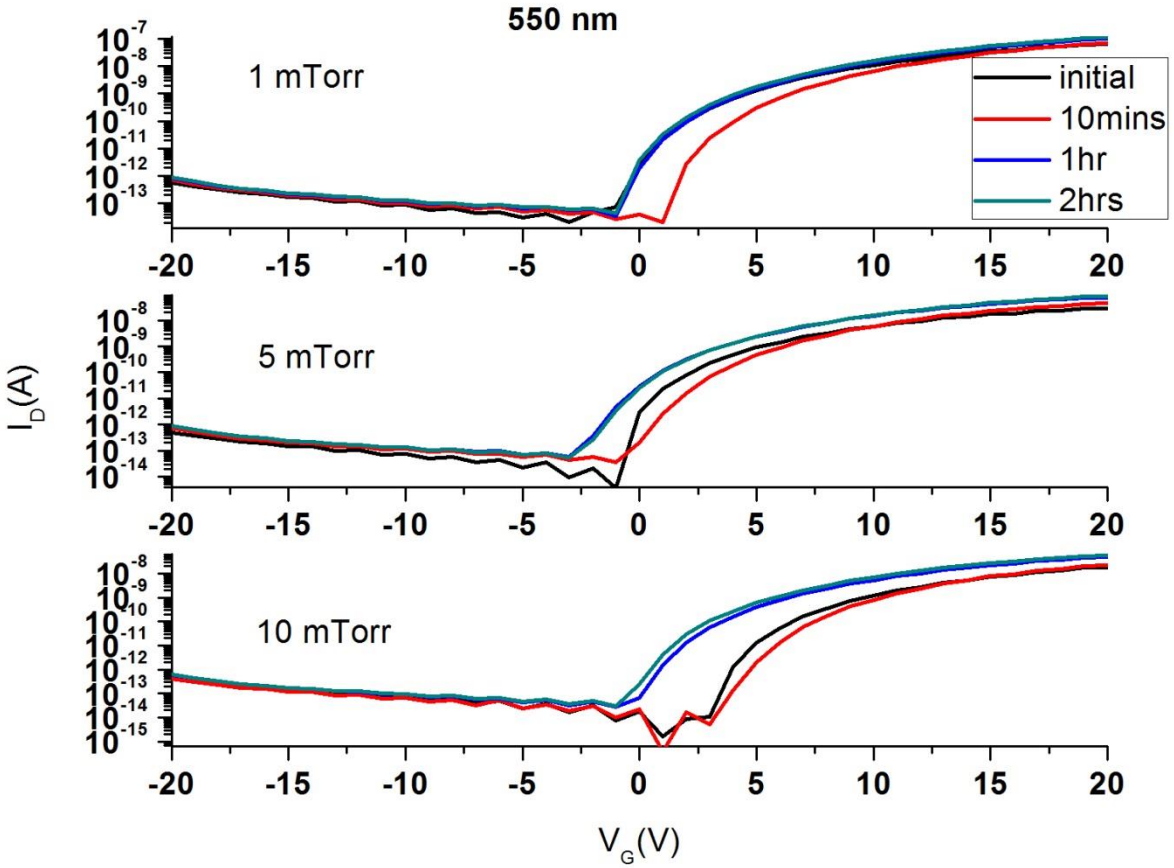

Figure 78 I-V transfer plots of 550 nm photo stability results as a function of duration.

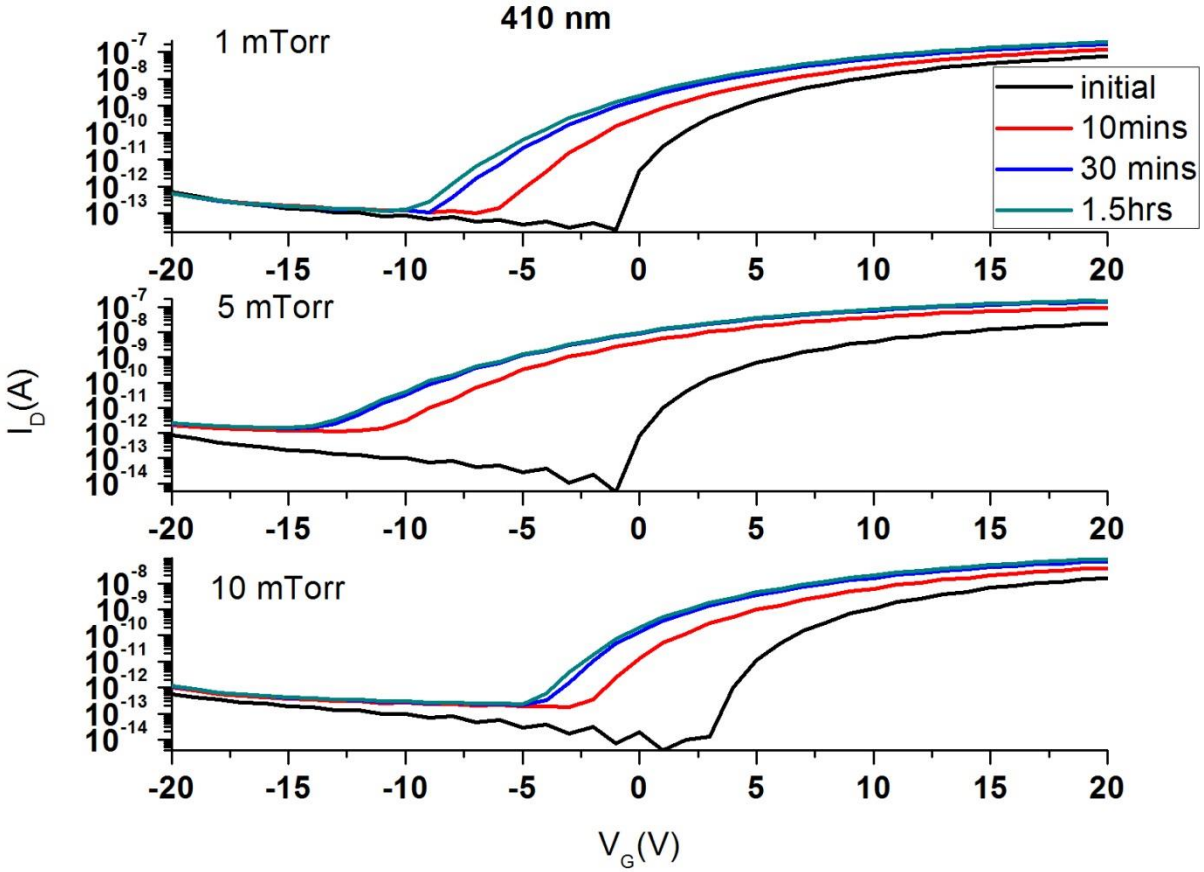

Figure 79 I-V transfer plots of 410 nm photo stability results as a function of duration.

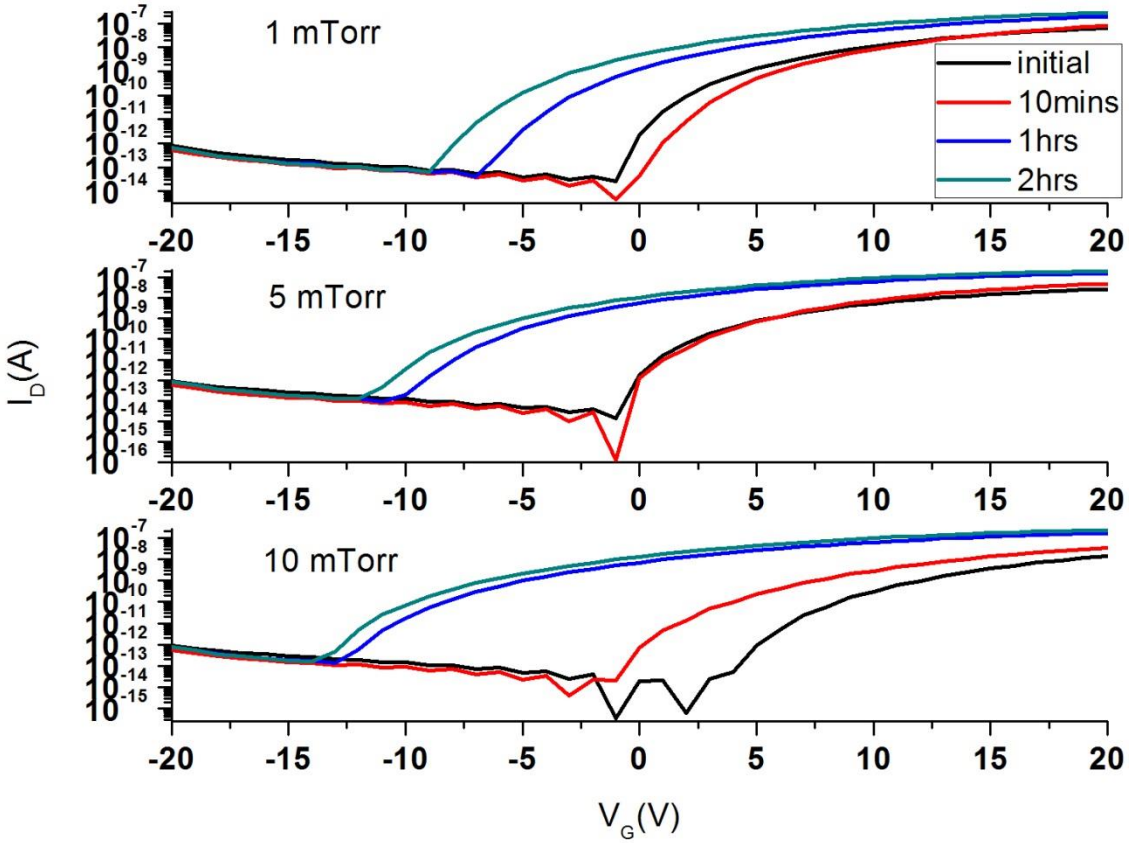

Figure 80 I-V transfer graphs of NBIS stability tests on 1, 5 and 10 mTorr devices.

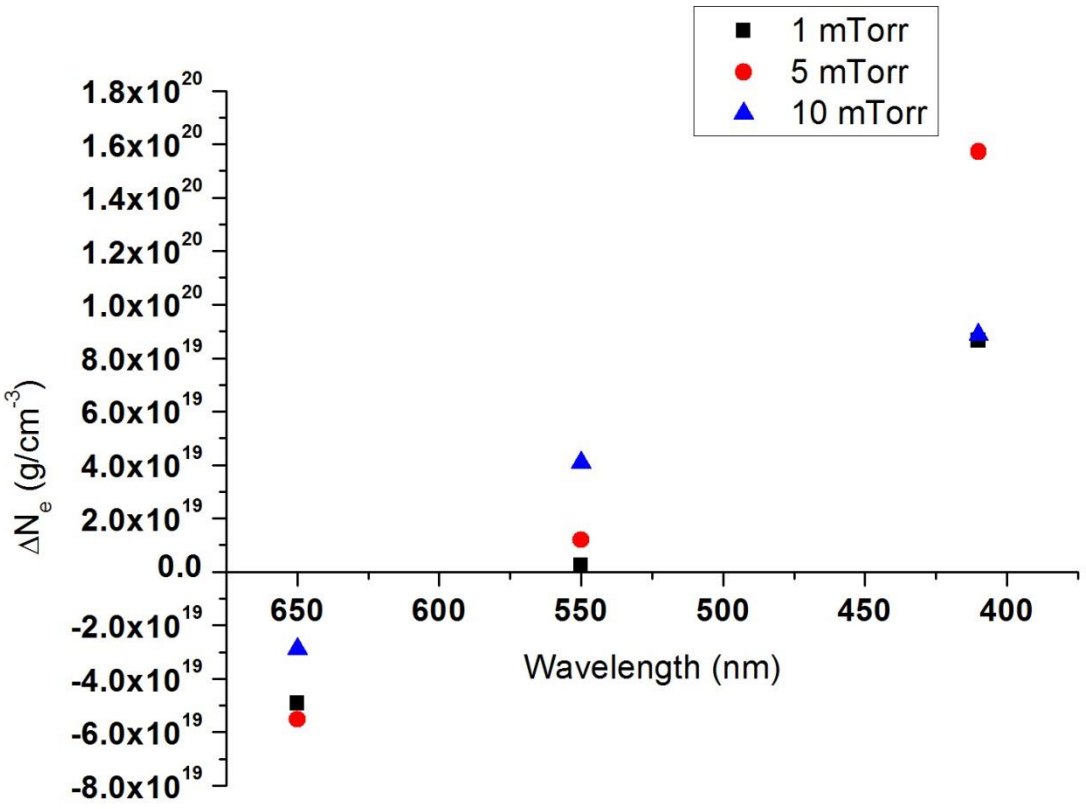

Figure 81 Change in carrier concentration after optical stability measurements

Figure 82 show the C-V measurements taken on samples optically stressed with 650 nm for 1 hour, 550 nm for 2 hours and 410 nm for 1.5 hours as well as the 550 nm NBIS device for 2 hours. It can be seen that the accumulation capacitance for the 650 nm stressed devices is the highest for the 1 mTorr device and reduced for the 5 and 10 mTorr device. However the order is reduced as the accumulation capacitance is lowest for the 550 nm stressed 1 mTorr device as compared to the 5 and 10 mTorr devices. For all devices, the accumulation capacitances of the 410 nm stressed and 550 nm NBIS are similar.

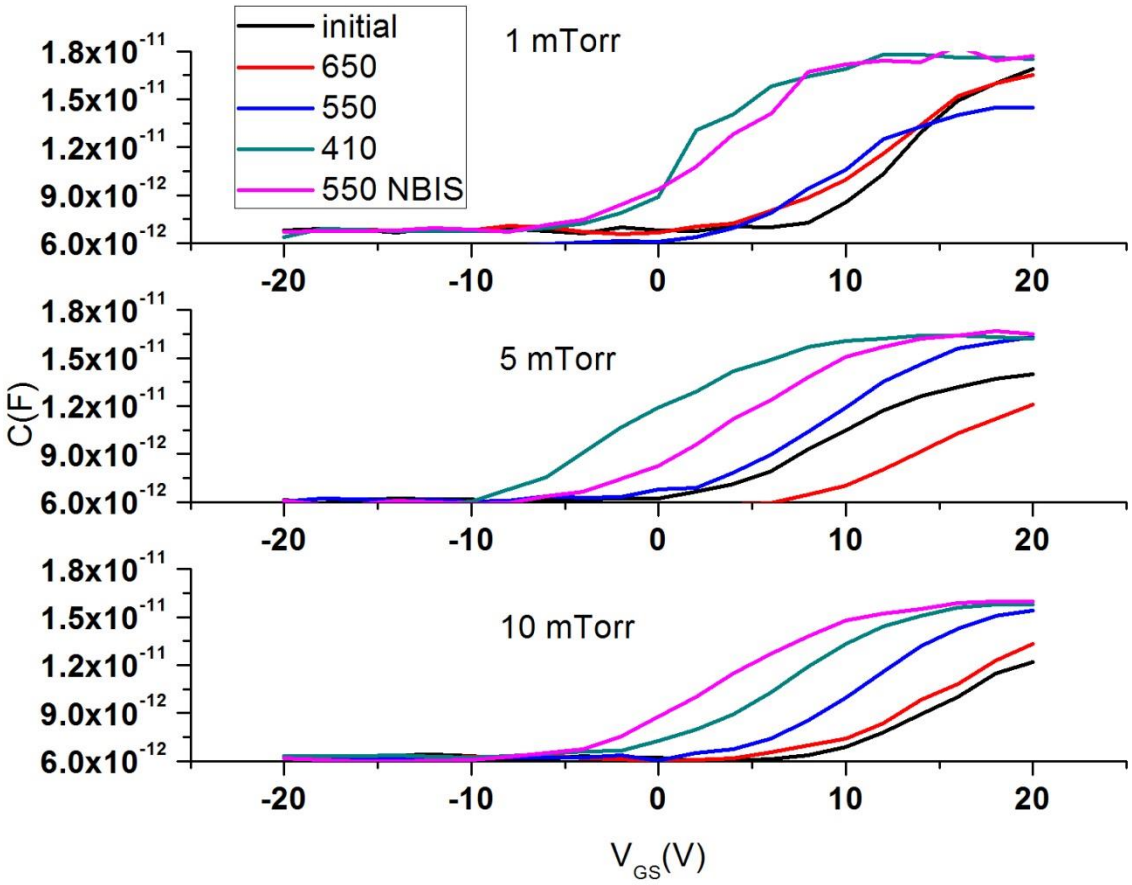

Figure 82 C-V plots of pressure dependent devices under photo-illumination

Figure 83 show the 15 V positive bias stress (PBS) measurements taken on devices deposited at 1, 5 and 10 mTorr pressures. The 10 mTorr device showed the lowest positive shift of ΔV_{ON} (~0.75 V) while ΔV_{ON} increases for the 5 mTorr and 10 mTorr devices (~8.3 V and 12 V). I_{OFF} and SS remained invariant for all devices. Devices were again tested after 72 hours and it can be shown that all devices shifted nearly towards their original states. PBS and recovery time measurements were taken on the selected 5 mTorr device to examine recovery time (*Figure 84*). It can be seen that 20 minutes after stressing for 3 hours, device performance began returning to its original characteristics. After 7 days it can be seen that the device is near its original state.

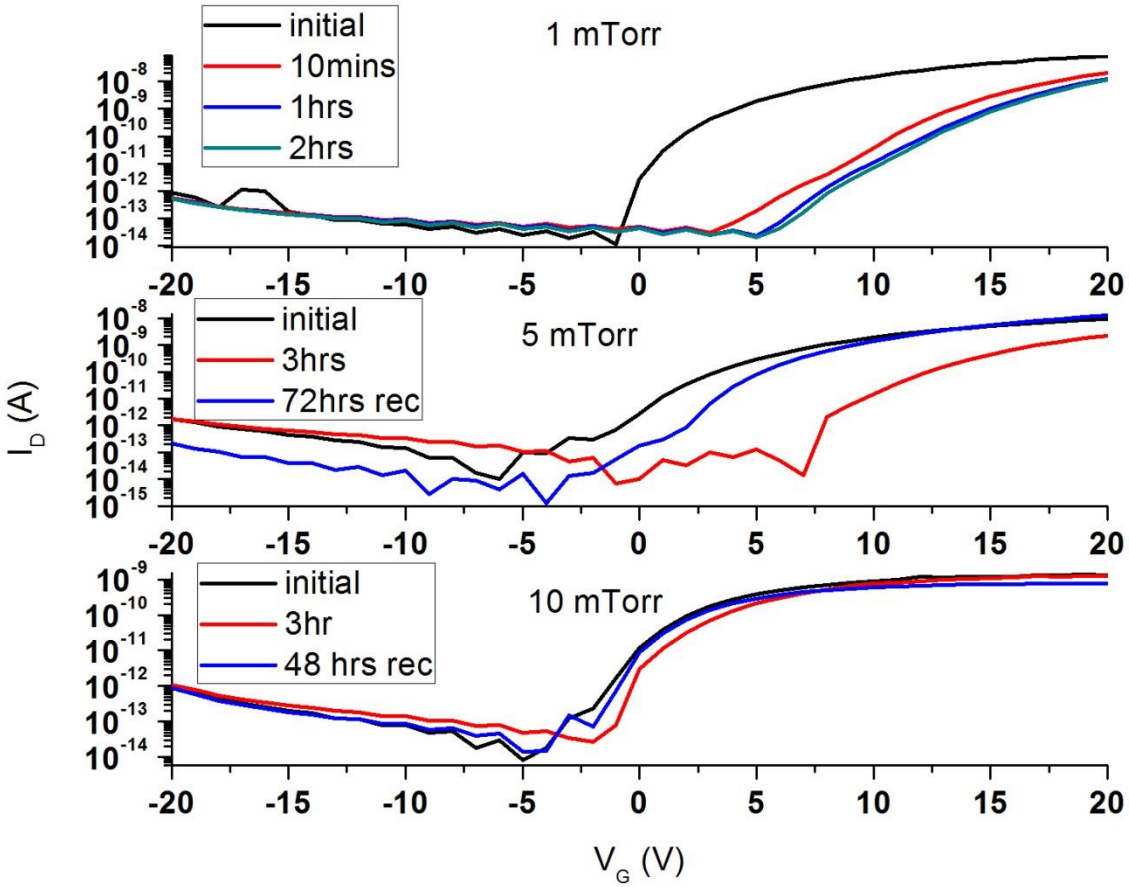

Figure 83 I-V plots of pressure dependent devices under positive bias stress

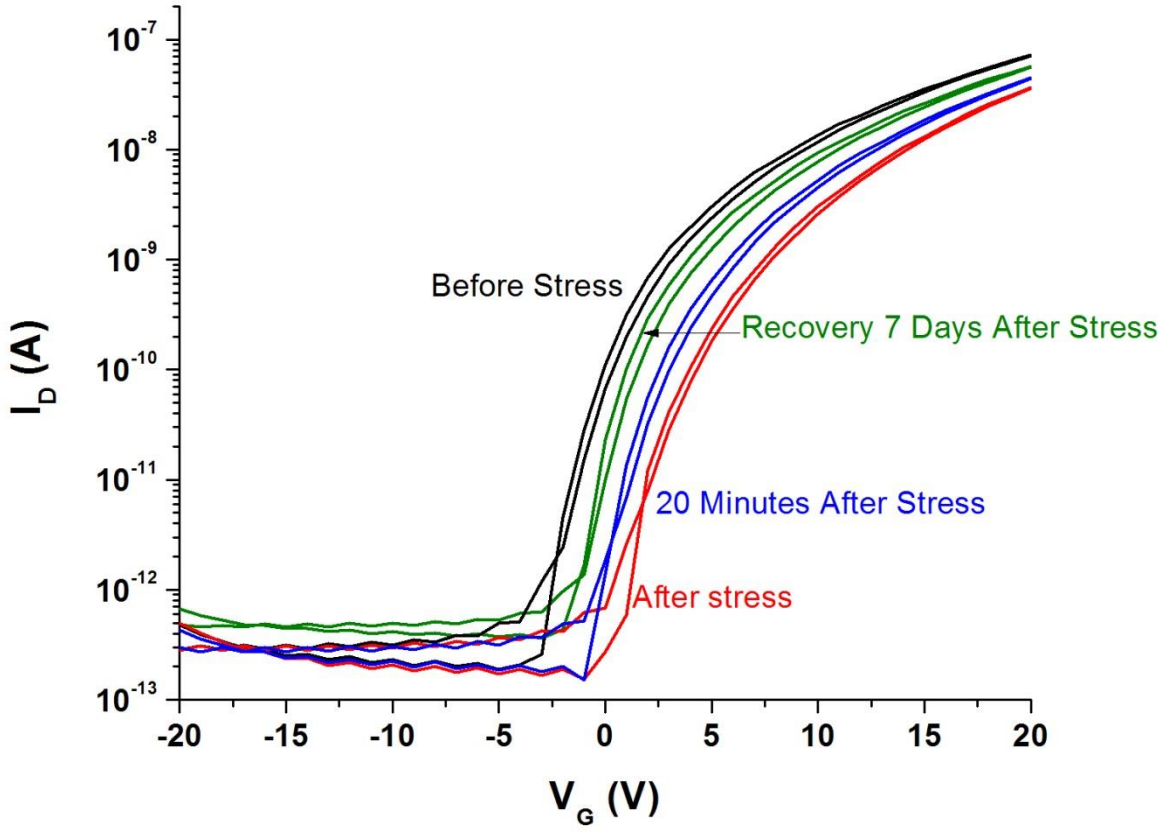

Figure 84 PBS and recovery time measurements taken of the 5 mTorr GSZO TFT

6.7 Conclusion

In summary, pressure-dependent GSZO TFTs and thin films were investigated to gain insight into the effect of deposition pressure on the morphological and compositional properties of the films as well as the electrical performance and optical stability of the devices. It can be seen that with increasing deposition pressure V_{ON} shifts positively and reduces in carrier concentration with the largest hysteresis in I-V and C-V plots being exhibited in the 10 mTorr device. C-V plots show an increase in V_{FB} with increasing deposition pressure with an overall increase in capacitance for the 10 mTorr device. Film porosity and surface smoothness increases with deposition pressure as shown from XRR and AFM data. XPS analysis showed all films to

have similar composition on the surface however major changes take place just 5 nm below. Photo-stability measurements showed the 10 mTorr to be most stable at 650 nm stress and the 1 mTorr film to be most stable at 550 nm and 410 nm. PBS characterization showed the 10 mTorr device to be most stable with minimal change in V_{ON} after 3 hours.

CHAPTER 7

Discussion

In this chapter, a discussion of all reported results in chapters 5 and 6 is presented while providing a cohesive explanation. Section 7.1 discusses what was reported on TFTs with 50 °C deposited films while section 7.2 discusses for 100 °C devices. Effects such as annealing temperature, annealing duration and channel thickness are discussed. Also discussed are the variations in device characteristics with GSZO films deposited under different deposition pressures. Variation in I-V and C-V characteristics along with composition, optical and electrical stability are discussed and correlated to determine the prevalent carrier transport mechanisms that control the device performance. Lastly, devices fabricated on PEN are discussed, examining the effects of gate oxides and the su-8 planarization layer.

7.1 50 °C Deposited Films

Continuing the research of work from our earlier group [21], subsequent 30 nm films were deposited at 50 °C in a 5 mTorr deposition pressure. Our previous reports on GSZO films were annealed at 250 °C which is too high a temperature to fabricate TFTs on PEN. Therefore the effect of reducing the annealing temperature was examined by annealing GSZO films at 140 °C for 1 hour and fabricating bottom-gate TFTs. Next we examined the effect of different annealing durations on the electrical and morphological properties of the GSZO films and devices.

7.1.1 Lower Annealing Temperature TFTs with GSZO films annealed at 250 °C have been compared to GSZO TFTs annealed at a lower temperature of 140 °C (Table 5) to examine the deleterious effects of lowering annealing temperatures. Overall device performance degraded with the lowering of the annealing temperature, showing a reduction in $I_{ON/OFF}$ and I_{ON} by 1 order

of magnitude and an increase in SS x4. Such a large increase in SS is either associated with either a dense increase in carrier concentration or D_{IT} [45]. Since the 140 °C device showed a decrease in I_D by an order of magnitude it is reasonable to assume that the lower annealed GSZO film has a higher concentration of D_{IT} than the 250 °C. Low quality film adhesion and high density defects are believed to be the source of device degradation since it is well-known that increasing annealing temperature improves adhesion of the semiconductor/insulator interface along with local atomic rearrangement and metal bonding [34].

7.1.2 Annealing Duration To sustain low annealing and processing temperatures suitable for flexible substrates, the effect of longer annealing duration was examined (Table 6 and Figure 26). The results clearly indicate improvement in the TFT performance with an improvement in I_D and $I_{ON/OFF}$ an order of magnitude with a minimal effect on $I_{OFF.}$ SS improved by reducing by half and an increase in μ_{FE} by 2 orders of magnitude. Increased channel conductivity caused a negative shift in V_{ON} from -2.5 V to -9.5 V which is the result of an increase in carrier concentration. This, in turn, is the cause of the enhanced the field effect mobility by 2 orders of magnitude. This is consistent with the commonly known characteristic within AOS layers [5] that an increase in carrier concentration results in corresponding increase in mobility. PCA devices showed an improvement in device performance with SS reducing to 2 V/dec and μ_{FE} increasing for each sample (Table 7). This improvement in device performance is likely due to an improvement in film adhesion at the GSZO/SiO_2 interface since the devices were placed directly on a hot plate [46]. Significant reduction in the hysteresis of the transfer characteristics with annealing duration (Figure 48) reveals the decrease in trap density at the semiconductor/insulator interface [47].

XPS analysis shows annealing duration to have very little effect on the atomic composition of the film however an increase in Sn^{4+} at.% can be seen in devices with GSZO films annealed for 10 hours (Table 10 and Figure 29-Figure 30). This shows that along with increasing annealing temperature, longer annealing durations cause an increase in Sn^{4+} at.% due to local rearrangement of O atoms near Sn^{2+} atoms causing a change in oxidation state to Sn^{4+}. The binding energy 484.5 eV can be attributed to the metallic Sn^0 atoms which are known to increase the conductivity of ZnO based films [48]. Though it can be seen from Table 21 that increasing annealing temperatures removes Sn^0, annealing duration of 10 hours still has traces of the Sn^0 metal indicating lack of energy needed by oxygen atoms to migrate to nearby metal cation. The above improvement in the TFT parameters in conjunction with invariant I_{OFF} strongly suggests that both longer annealing is effective in annihilating only the shallow traps.

7.2 100 °C Deposited Films

All subsequent GSZO films were deposited at 100 °C in preparation for GSZO TFTs. A comparison of 50 °C and 100 °C was taken to examine the electrical and compositional effects by increasing the deposition temperature. TFTs with GSZO films of different thicknesses were fabricated to investigate the electrical and morphological properties as film thickness increases. Finally we investigated the effects of high-temperature annealing by comparing low-temperature TFTs annealed at 140 °C to high-temperature TFTs annealed at 450 °C since high-temperature annealed TFTs yielded better TFT performance.

7.2.1 Low-Temperature Deposition vs. High-Temperature Deposition Increasing the deposition temperature from 50 °C to 100 °C provided an improvement in device performance due to the enhancement in I_D by an order of magnitude and $I_{ON/OFF}$ by 2 orders of magnitude however V_{ON} shifted negatively by ~4 V and SS slightly degraded to 0.7 V/dec (Table 11 and

Figure 31). From these it is evident that an increase in deposition temperature caused an increase in carrier concentration which is the cause of the changes in device performance. This increase in carrier concentration is likely due to the concentration of Sn^0 in the bulk of the 100 °C deposited film since it is known to increase carrier concentration. The high concentration of Sn^0 coupled with the Sn^{4+} at.% are likely causes of the improvement in μ_{FE} since Sn^{4+} has the $[Kr](4d)^{10}(5s)^0$ electronic configuration needed to improve electron mobility.

Increasing the deposition temperature from 50 °C to 100 °C had little effect on the bulk atomic composition (Table 12) however traces of hydroxyl (O-H) molecules can be found in the bulk of the 50 °C film. An increase in Sn^{4+} at.% can be found in both the surface and bulk of the 100 °C film, likely causing an improvement in device performance since Sn^{4+} has the $[Kr](4d)^{10}(5s)^0$ electronic configuration needed to improve electron mobility.

7.2.2 Comparison with Higher Annealed Temperature Device Using this optimized deposition temperature we have attempted to compare the low annealed temperature device with the device fabricated with the channel annealed at higher temperature of 450 °C to ascertain if there is any valence change in the elements or coordination that is responsible for the observed large differences in these two sets of devices (Table 18-Table 21 and Figure 43-Figure 47). Characterization was performed on films annealed at 140 °C and 450 °C to examine the effects of annealing temperature on atomic percentages. XPS characterization show a slightly less O-rich oxide surface layer with annealing temperature reduction however more O-rich in the bulk of the film. There appears to be very little change in Ga at.% and Sn at.% with annealing temperature reduction. OI (530.2 eV) is attributed to the oxygen bound with cations, OII (531.7 eV) is attributed to O^{2-} ions in oxygen-deficient regions and OIII (532 eV) is usually attributed to the presence of loosely bound oxygen on the surface of the GSZO film, belonging to a specific

species, e.g., –CO , adsorbed H-O or adsorbed O within the amorphous film [49]. The de-convoluted O 1s spectra peaks show a decrease in OI at.% and an increase in OII at.% with decreasing annealing temperature. The OIII at.% is a low percentage on the surface of the film however it vanishes within the bulk. As stated above, these are loosely bound O-related defects usually absorbed onto the surface of the film and are not seen within the bulk. The increase in OII at.% with decreasing annealing temperature shows an increase in oxygen vacancies (V_O) which is expected since oxygen interstitials (O_I) do not have sufficient thermal energy to migrate and fill such vacancies [50]. Many of these V_O's can be shallow defect locations (V_O^{2+}) which are known to capture electrons from the conduction band (CBM) and degrade device performance which can be seen Table 18. XPS characterization show a high density of Sn^{4+} on the surface of both films however this concentration is significantly reduced in the bulk of the 140 °C film. Since the films were annealed in air and it is well known that Sn^{4+} is created by the migration of O atoms to nearby Sn^{2+} ions [22], it is understandable that a higher concentration of Sn^{4+} can be seen on the surface and reduces within the bulk. Since decreasing annealing temperature causes less atomic rearrangement in the film it is less likely that nearby O atoms will cause Sn^{2+} to become Sn^{4+} [51]. It is not understood why traces of the metallic Sn^0 can be found on the surface of the film however they are quickly oxidized once annealed in air likely due to oxygen absorption. Thus higher concentration of Sn^{4+} configuration is responsible for the superior characteristics exhibited by the TFTs annealed at higher temperatures.

7.2.3 Channel Thickness TFT performance (Table 15-Table 16 and Figure 36-Figure 39) also improved with the reduction in the channel thickness as shown in section 5.4, which is discussed in the following.

(a) Improvement in SS, μ_{FE} and I_{OFF}:

First, the active channel layer thickness extends only up to a couple of nm from the gate oxide/active channel interface; and secondly, the thinner channel layer is more dense and exhibit smoother interface as inferred from XRR data Table 15, leading to improved SS and carrier mobility. Hence the additional bulk channel layer in a thicker channel impacts the TFT performance only adversely by contributing to the background carrier concentration resulting in a large negative V_{ON} shift with enhanced I_{OFF}. This increase in I_{OFF} can also be inferred from Equation 6 where I_{OFF} is proportional to channel thickness, t_{CH} [52].

$$I_{OFF} = \frac{t_{CH} W \sigma V_{DS}}{L} \qquad \text{Equation 6}$$

(b) Positive shift in V_{ON} close to the origin and reduction in I_D:

Furthermore, the surface sensitivity to the oxygen adsorption from the ambient forming different strongly bonded negative ionic species such as O2-, O- etc and aids in creating the depletion region at the surface. In a thinner channel this represents a significant portion of the channel layer, thereby restricting the channel conductivity. This explains the decrease in drain current observed for lower channel thickness. Hence fully depleted region is formed readily in the thinner channel for small gate voltages thus leading to positive shift in V_{ON}. This is also further attested by the C-V profile variation with channel thickness Figure 37, namely a positive shift in the C-V characteristics accompanied with a sharper transition between the different regions of operation and enhanced accumulation capacitance with thinner channel. RBS characterization show very little change in atomic composition with channel thickness.

Though most of the behavior of GSZO TFTs with annealing and deposition temperature are similar to those observed in IGZO TFT, the salient difference between the two systems seems

to lie in the quality of the channel layer at lower thickness. Lower channel thickness in GSZO seems to result in denser layers and smoother interfaces, while IGZO reports seem to be unclear [53, 54]. Thus the lower thickness seems to be potentially more advantageous in the case of GSZO TFT.

PCA tests provided improvements in V_{ON} for the 20 nm and 10 nm devices by exhibiting positive shifts. This is likely due to the dehydration of adsorbed water at the surface and within the film [55]. The negative V_{ON} shift of the 30 nm device is due to the increased background carrier concentration which increases with channel thickness. This is evident in the increased I_{OFF} for the 30 nm device which degraded the $I_{ON/OFF}$ ratio. Since it is understood that SS is negatively affected by increased carrier concentration, as device thickness decreases, the SS improves thus suggesting carrier concentration to be dominantly effected by PCA.

Though the overall performance of GSZO transistor with processing temperature under 150 °C is still inferior to those obtained in the IGZO based TFT however an improvement has been made and there is a potential for further improvement by fine tuning of the processing parameters as well as the target composition and possibly a passivation layer.

7.3 Pressure Dependence:

TFTs with GSZO active layers deposited at different chamber pressures were compared to examine its effect on device performance. An in-depth systematic analysis was performed to study the electrical, morphological, compositional and optical properties of the GSZO films and devices. These films were 15 nm thick, deposited at 1, 5 and 10 mTorr deposition pressures and annealed at 140 °C for 3 hours.

7.3.1 I-V and Structural

(a) 1 mTorr device:

The 1 mTorr device showed the largest I_{OFF}, I_{ON} and most negative V_{ON} suggesting the film to be highly conductive. This can be verified by the devices large I_{OFF} from Equation 1 where t_{CH} is the GSZO channel thickness, W is device width, σ is film conductivity, V_{DS} is the voltage between the drain and source electrodes and L is device length [56]. Due to the high conductivity of the film, the carrier mobility [51] of the device was also the greatest at 0.43 $cm^2/V{\cdot}s$ with poor SS (1.8 V/dec) as it is well known that higher mobility is associated with higher carrier concentration [22] and SS is poor for higher carrier concentration and trap density [45]. XRR revealed a highly porous film for the 1 mTorr active layer as compared to the other films. Figure 65-Figure 67 shows AFM images (1 μm x 1 μm) of the surfaces of GSZO films deposited at different deposition pressures. The R_{rms} values decrease from 35.4 pm to 19.7 pm with increasing deposition pressure. The surface of the film deposited at 10 mTorr was relatively smooth with small aggregates. The 1 mTorr film had the highest surface roughness which was probably due to the high bombardment energy of the ions during channel formation which gives rise to a higher concentration of defects and O-H contaminants. Both the 5 mTorr and 10 mTorr films have skew and positive kurtosis indicating that the surface is more planar with predominant valleys and smoother peaks. The 1 mTorr film has a positive skew with a negative kurtosis indicating a surface with more peaks than valleys. This AFM data agrees with the XRR surface density data in that the 1 mTorr film is more porous with large roughness and sharp peaks. The 1 mTorr TFT is also most sensitive to air showing largest ΔV_{ON} after 2 months.

(b) 5mTorr and 10mTorr devices:

V_{ON} shifted positively with increasing deposition pressures going from -16 V to -1.8 V from 1 to 5 mTorr. A decreased I_{OFF}, I_{ON} and μ_{FE} were also observed suggesting the film is less conductive than the 1 mTorr film (Equation 3). Device performance improved as SS reduced

from 1.8 V/dec to 1.1 V/dec, $I_{ON/OFF}$ increased from $7.4x10^5$ to $4.7x10^6$ and ΔV_{ON} decreased from 1.3-0.9 V. This suggests a reduction in CB tail states [22] and a further reduction in I_{OFF} than I_{ON} as the deposition pressure decreased. At 10 mTorr I_{OFF} and I_{ON} also decreased with $I_{ON/OFF}$ increasing even further to $5.2x10^6$ suggesting a less conductive film than the 5 mTorr and improvement in device controllability. The mobility of the 10 mTorr film improved however which is most likely due to the increase in film density which reduces Vo. However the 10 mTorr device showed the greatest hysteresis of 2 V suggesting a large density of traps in the active region of the GSZO layer [57]. This large hysteresis was also observed in the C-V curves shown in Figure 64. The large density of traps is believed to be due to the high density of oxygen vacancies which are occupied which form deep states as will be inferred later from stability measurements.

Due to the increased channel density of the 10 mTorr film as well as smooth interfaces determined from XRR measurements in comparison to the 1 and 5 mTorr (Table 25), it is speculated that the electrical permittivity of the oxide is larger in this 10 mTorr device leading to the observed increase in capacitance in both the depletion and accumulation regions. This is found from Equation 7 where ε is the films electrical permittivity, A is the area of the GSZO film and t_{CH} is the thickness of the GSZO layer.

$$C = \frac{\varepsilon A}{t_{CH}} \qquad \text{Equation 7}$$

I_D saturation improved with increasing deposition pressure which is likely due to control of carriers within the film (Figure 59). The 5 mTorr film exhibits the sharpest slope in C-V curves along with the smallest hysteresis suggesting the film has overall less trap states.

7.3.2 Compositional Characterization

a) 1 mTorr and 10 mTorr:

XPS characterizations show the surfaces of both the 1 and 10 mTorr films to be relatively similar with Ga and Sn at. % are relatively low constituting less than 6 % of the film. Traces of the loosely-bound hydroxyl molecules exist both on the surface and within the bulk of the 1 mTorr device. Since hydroxyl molecules acts as donors and passivate defects it is believed that this is the cause for the high concentration of carriers within the 1 mTorr film. The 10 mTorr film had a large at. % of Sn^{4+} in the bulk which would then enhance the percolation conduction through distributed potential barriers around the conduction band edge and improve μ_{FE} [58]. This also explains why the 10 mTorr film has the larger optical gap from absorption measurement data (Figure 75) [12]. All devices showed transparency ≥80 % as shown in *Figure 76*.

b) 5 mTorr:

A relatively large atomic concentration of oxygen related defects was observed within the bulk of the 5 mTorr film suggesting the cause of the films 10^6 $I_{ON/OFF}$. However the 5 mTorr film also has the smallest SS and hysteresis which suggests low D_{IT} at the semiconductor/insulator interface. Therefore it is believed that these oxygen-related defects are V_O defects constituting deep levels. Being below the Fermi level as shown in *Figure 86* they do not affect the mobility of the device [58]. The 5 mTorr film shows higher concentration of Sn^{2+} in the bulk of the film which has been reported to introduce CB tail states and hence suggesting this to be the cause of the low mobility.

After 2 months of exposure to air, a change in device performances was observed. The 1 mTorr device showed a large increase in I_{OFF} resulting in a decrease in $I_{ON/OFF}$. Since the 1 mTorr device is more porous than the other devices as shown from XRR characterization (Table 25), this device is more susceptible to absorption of H_2O from the atmosphere. It is well known that

H acts as a donor to ZnO based films which would increase the conductivity of the film thus raising I_{OFF} [47]. The 10 mTorr device also showed an increase in I_{OFF} however not as much as the 1 mTorr device. XRR analysis shows the 10 mTorr device to be much denser than the 1 mTorr device resulting in little effect on the devices I_{OFF}. The 5 mTorr device showed a decrease in both I_{ON} and I_{OFF} resulting in no change in $I_{ON/OFF}$. Since a decrease in film conductivity was observed, it is believed the 5 mTorr film absorbed more O_2 than the other devices since they suppress carriers in the active layer [59]. XPS analysis reveals the 5 mTorr device to have the most V_O's in the bulk thus making it more susceptible to oxygen absorption. All device showed a dramatic decrease in hysteresis which shows the suppression of CB tail states which has been shown to be the cause of absorbed H atoms [47]. Therefore it was observed that the 5 mTorr device showed least sensitive to air exposure.

7.3.3 Optical Stability

a) 650 nm:

Pressure dependent devices were stressed with light illumination at 650 nm, 550 nm and 410 nm wavelengths for different durations to examine their optical stability. After applying 650 nm light on the active layer of the GSZO TFTs the 1 mTorr and 5 mTorr devices showed a similar positive shift in V_{ON} (~4.2 V) after just 10 minutes and remained stable even after 1 hour while the 10 mTorr device showed a smaller V_{ON} shift of 2.5 V (Figure 77). The 650 nm light has photon energy of ~1.91 eV which excites electrons trapped in the CB tail states and shallow traps but is too low of energy to excite charges from deep traps as shown in *Figure 86*. Since a positive shift in V_{ON} constitutes a net decrease in electrons within the film it is believed that more charges are being trapped than generated and after 10 minutes a stable balance where the rate of charges trapped equals the rate of charges generated. This suggests that shallow light

induced electron traps are generated. The 10 mTorr device is shown to have smallest ΔV_{ON} suggesting that the light induced traps are influenced by the quality of the channel and the interface leading to less total density of traps for less defective film and smoother interface as attested by XRR and XPS in 10 mTorr device. I_{OFF} is invariant for all devices which is expected since the deep traps are not expected to be activated at this wavelength. C-V measurements show a larger capacitance for the 1 mTorr device than the 5 mTorr and 10 mTorr devices most likely due to the large channel conductivity in the 1 mTorr device. There is a gradual increase in V_{FB} with increasing deposition pressure consistent with the Von shift observed in I-V measurement. The slope of the C-V characteristics in the transition between the accumulation and depletion regions10 mTorr device is shown to be higher than the 1 mTorr and 5 mTorr devices attesting to the lower concentration of traps excited at 650 nm wavelength as concluded earlier from I-V data.

b) 550 nm:

Unlike reported in literature [60], the illumination of green light (550nm) on GSZO TFTs (Figure 78) caused a positive V_{ON} shift within 10 minutes. However, these devices gradually shift negatively thereafter, but the ΔV_{ON} remained stable after 1 hour. This is attributed to the following process: 1) the charges being trapped outnumber the photo-generated charges within the first 10 minutes, and 2) the trap states being filled and the photo-generated charges increases the carrier concentration and shifts V_{ON} negatively. The 1 mtorr device has the largest initial positive shift and then return to its original state with no significant change in SS indicating a low density of deep traps. However, the 5 and 10 mtorr continuously shift negative afterwards. The 10 mTorr device showed the largest negative V_{ON} shift of ~5 V. I_{OFF} remained invariant

while SS slightly degraded for the 5 mTorr and 10 mTorr devices. This suggests the 10 mTorr device has a large density of deep traps.

The 550 nm light has photon energy of ~2.25 eV which excites electrons trapped in the CB tail states, shallow traps, mid traps as well as lower-energy deep traps as shown in *Figure 86*. I_{OFF} remained invariant while SS slightly degraded for the 5 mTorr and 10 mTorr devices. This suggests the 10 mTorr device has a large density of deep traps while the 1 mTorr device has a low density of deep traps, enough to return to its initial state and remain stable.

It is well known that deep traps in ZnO alloy films mainly consist of neutral V_O's with filled states, which require ~2.3 eV to excite 2 electrons into the CBM resulting in interface trap density, D_{IT}, a shallow level close to the conduction band associated with V_O^{2+} [61]. Thus for every 2 electrons generated, an interface state density D_{IT} is created. These electrons generated from the deep trap at this wavelength explain the subsequent negative shift observed in all films. This is also consistent with the changes in SS observed only in the 5 mTorr and 10 mTorr devices indicative of increased D_{IT} and the dominance of V_O transition. C-V data is also consistent in that the 1 mTorr device shows the lower C_{acc} as compared to the other devices indicative of comparatively decreased conductivity in this device. Based on the data it appears the 10 mTorr devices have the highest density of deep traps leading to largest number of V_O to V_O^{2+} transitions.

c) 410 nm:

Devices stressed with 410 nm wavelength light showed a negative shift in V_{ON} within 10 minutes accompanied with degradation in both I_{OFF} and SS in all the devices. Again the magnitude of the changes observed were similar in 1mTorr and 10mTorr devices with the 5mTorr device exhibiting the largest degradation in device performance with a ΔV_{ON}=-12 V,

ΔSS=1.54 V/dec and the largest increase in I_{OFF} by an order of magnitude. C-V measurements show the 5 mTorr device to have a V_{FB} in the negative region accompanied with a large hysteresis and a small slope in the transition region between the depletion and accumulation regions. Since the 410 nm wavelength light has hυ= 3.02 eV which is in the vicinity of the VB tail states and not a significant change observed for 550 nm, it is indicative of the fact that these changes are not only due to deep traps but also valence band tail state, which has a much large density, particularly in 5mTorr device. Both the 1 mTorr and 10 mTorr devices show similar ΔV_{ON}, I_{OFF} and SS degradation suggesting the total density of traps within the band gap of these films are nearly the same however distributed differently. C-V measurements show the 1 mTorr device to have a larger capacitance with a fully formed accumulation region suggesting it has a higher carrier concentration than the 10 mTorr device which can be clearly seen from the I-V data. Since the other data from XRR, AFM and XPS show the 1 mTorr film to be most porous, rough and consisting of largest hydroxyl contaminants even 5 nm below the surface, this somewhat lower shift in V_{ON} as compared to 5nm could be due to the presence of large density of shallow interfacial electron traps and the carriers generated by 410 nm can also be trapped in these sites giving rise to positive V_{ON} and overall resulting in less shift. Thus 1mTorr appears to be more stable for λ<550nm illumination stress as it is dominated by shallow electron traps.

Figure 81 supports the theory above and shows the change in the films carrier concentration (ΔN_e) with optical stress wavelength, calculated from Equation 5, due to the density of electron traps and VB tail states within the bandgap of the films. All devices showed a reduction in Ne during the 650 nm stress which is clear by the positive shift of V_{ON} (Figure 77). This decrease in N_e is likely the cause of shallow defects within the bulk and at the semiconductor/insulator interface which trap free carriers. It can be seen that the 1 mTorr and 5

mTorr devices more easily trap charges than the 10 mTorr device suggesting a higher concentration of D_{IT} as shown in *Figure 86*. The 10 mTorr device showed the largest negative shift in V_{ON} thus indicating a large increase in N_e of the film. A wavelength of 550 nm constitutes a photon energy level of $h\upsilon$= 2.25 eV which is within the vicinity of deep traps (*Figure 86*) thus revealing deep traps as the primary cause of ΔV_{ON}. The 410 nm wavelength stress values show all devices to have negative shifts in V_{ON} (Figure 79) with the 5 mTorr device being more prominent. The corresponding energy level ($h\upsilon$=3.02 eV) is in the region of deep states and VB tail states. Since I_{OFF} increased x100 for the 5 mTorr device this is likely due to the excitation from the VB tail states which contributed free carriers to the CB. A comparison of band gap states is illustrated in Figure 86.

7.3.4 NBIS NBIS characterization was carried out on the pressure dependent samples with a 550 nm wavelength light and a -15 V gate bias for 2 hours. With 10 minute illumination, the V_{ON} shift varied from positive to negative with increasing pressure. Thus after 10 minutes a net decrease in carrier concentration exists in the 1 mTorr device indicative of large density of shallow traps in the films consistent with earlier observations. The 5 mTorr device showed no change in V_{ON} as the light induced electron traps seems to balance the charge-hole creation from deep traps. A large negative shift observed in the 10 mTorr device is indicative of the presence of large density of deep traps again consistent with earlier discussion. The contribution to the high conductivity in this case is not only due to the electron generation from the deep trap but also caused by the transport of Vo^{2+} towards the interface screening the gate bias resulting in an additional negative shift in V_{ON}. After 10 minutes V_{ON} shifted negatively for all the devices due to the above mechanism discussed, however the 10 mTorr device exhibited a much larger negative shift. This indicates that 10mTorr device performance has the highest deep trap density

as the 550 nm wavelength light does not excite carriers from the VB tail states. The SS degraded and I_{OFF} increased due to the increase in carrier concentration for all devices. This is also reflected in the similar C-V characteristics observed when measured at the end of the bias stress. Amongst these three devices the 10 mTorr device exhibited highest instability under NBIS with 550 nm light due to large density of deep traps.

7.3.5 PBS Positive bias stress measurements showed a gradual decrease in ΔV_{ON} (1 mTorr-12 V, 5 mTorr-8.3 V and 10 mTorr-0.75 V) with increasing deposition pressures. The positive shift in V_{ON} is due to the trapped carriers exceeding the photo-generated carriers. The dominance of trap over the free carrier generation is due to low illumination intensity used. The more porous 1 mTorr device showed the largest positive V_{ON} shift suggesting it has the highest concentration of shallow electron traps. This density of shallow electron traps decreases with increasing resulting in a much more stable GSZO TFT with a ΔV_{ON} of only 0.75 V at 10 mTorr deposited device. The 1 mTorr device also shows a hump in its electrical characteristics which has been reported to be the presence of Zn_I which forms a second path of charge flow [44]. The porous nature of the 1 mTorr device further allowed the mobility of Zn_I to the surface of the film after PBS which thus formed the second current path (Figure 85). The presence of this hump is slightly seen in the 5 mTorr device however cannot be seen in the 10 mTorr device. A gradual increase in film density with deposition pressure from XRR data explains this gradual reduction of hump presence in the transfer I-V characteristics. The higher deposition pressure improves the stability of GSZO TFTs under PBS.

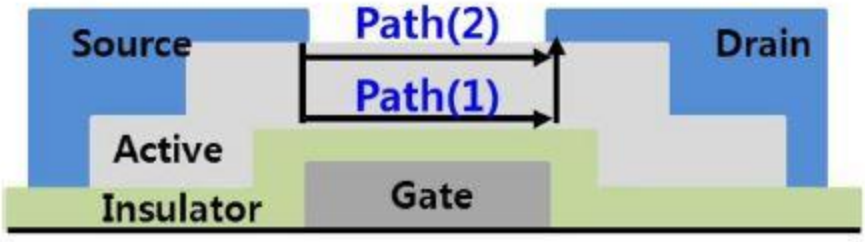

Figure 85 Schematic cross section of the TFT with two parallel current paths under the constant gate bias stress due to the presence of Zn_I [44].

In our group Briana et al. [62] in order to characterize the bias-stress effect, the measure of decay and recovery under an applied positive gate and negative bias was estimated using Equation 8:

$$\Delta V_{ON} = \Delta V_{ON_0} \{1 - (\exp(-(t/\tau)^{\beta}\} \quad \text{Equation 8}$$

where ΔV_{ON_0} is the ΔV_{ON} at infinite time, β is the stretched-exponential exponent, and τ is the trapping time for the stress phase and detrapping time for recovery phase. The τ has been associated with the duration for which the electrons are trapped or the average time for oxygen adsorption. In our case, the following results can be better explained when τ is considered as the duration associated with the trap rather than oxygen adsorption.

The experimentally obtained results were well fitted by the stretched exponential equation. The obtained fitting parameters, τ and β, for the pressure-dependent TFTs were 1.1 x 10^2 s and 0.4 for stress phase and 1.0 x 10^3 s and 0.58 for the recovery phase, respectively. Observed trends showed a decrease in τ with an increase in pressure and increased annealing temperature (450°C ~10^1) than at 140°C (~10^2) by 1 order of magnitude. A smaller τ means long term stability. This suggests that post annealing treatment at higher annealing temperature and higher pressures improves the stability of a GSZO thin films electrical characteristics.

Based off stability tests it is believed that low pressure 1 mTorr device contain less deep traps and is stable during low-wavelength stability tests while the 10 mTorr device is stable during electrical stability and high wavelength tests and the 5 mTorr device is unstable for both optical and electrical stress tests. Figure 86 shows a depiction of the energy band diagrams of each device which illustrates the density of traps at individual energy locations within the forbidden band gap.

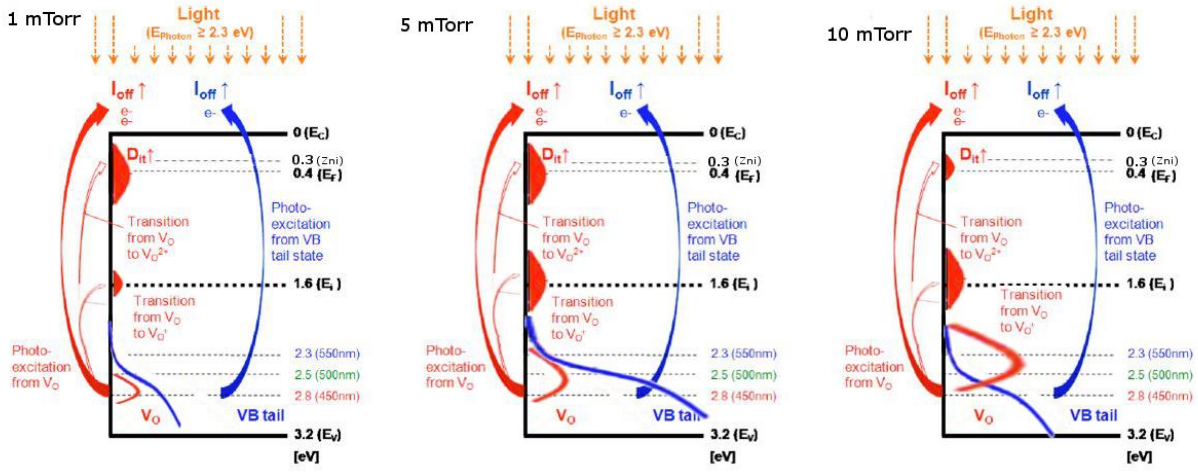

Figure 86 illustrates the energy band diagrams of the 1, 5 and 10 mTorr GSZO films.

7.4 Bottom-Gate GSZO TFT on PEN Substrate

In collaboration with RTI International, bottom-gate TFTs were fabricated on PEN with the optimal a-GSZO film after the preceding electrical, optical, structural and atomic characterizations. TFT-A had a PECVD SiO_2 layer as the gate oxide, TFT-B had a Si_3N_4 gate oxide, TFT-C had Si/su-8/Si_3N_4 and TFT-D had PEN/su-8/ SiO_2.

TFTs A and B exhibit poor TFT performance with $I_{ON/OFF}$ ~10^2 and 10^3 with relatively large SS's of 8 V/dec and 5.4 V/dec. The substandard SS performance of the devices suggests a large density of shallow traps near the CBM. Also degrading the SS may be the high conductivity of the films (Equation 3) due to the relatively large I_{OFF} of 10^{10} and 10^{11} as

compared to devices on Si (~10^{13}) [45]. Devices C and D, which contained an su-8 planarization layer showed large improvements in $I_{ON/OFF}$ (10^5), SS (0.6 V/dec and 0.7 V/dec) and μ_{FE} (0.5 $cm^2/V \cdot s$ and 0.7 $cm^2/V \cdot s$). It is well known that su-8 serving as a planarization layer reduces surface roughness of the PEN and the PECVD deposited gate oxide [63]. This is likely the cause of the large improvement in μ_{FE} which is degraded with increased surface roughness scattering. Both devices show low I_{OFF} current near 0 V however I_D increases nearly 3 orders of magnitude upon negative V_{GS} sweep. This increase in carrier concentration is likely due to the presence of holes in the films since the gate insulators were PECVD grown instead of thermally oxidized TFT-D exhibited negative slope in saturation region of the I-V output characteristics suggesting a decrease in μ_{FE}. This is characteristic of the device where the temperature has increased as it occurs only for large currents with V_D and V_G approaching high voltages (15-20 V). The lower PEN thermal conductivity does not allow the dissipation of heat readily at high currents leading to the heating of the device and mobility degradation. To confirm, TFT-D was then tested with decreased time delay and the output saturation and indeed μ_{FE} degradation did not occur.

7.5 Conclusion

In conclusion low-temperature GSZO TFTs have been fabricated on plastic with electrical performance comparable to TFTs fabricated on n^+ Si. Channel thickness, deposition pressure and annealing duration have large effects on the performance of the devices. TFTs with 15 nm GSZO films deposited at an increased deposition temperature (100 °C), chamber pressure of 5 mTorr and annealing duration of 3 hours were shown to produce the best TFTs for plastic substrates. Bottom-gate TFTs on PEN with su-8 planarization layer produced good TFT performance comparable to IGZO TFTs ($I_{ON/OFF}$ ~10^5, SS ~0.7 and μ_{FE} ~0.7 $cm^2/V \cdot s$).

CHAPTER 8

Conclusion and Future Work

8.1 Conclusion

In this work a comprehensive study of the effects of deposition parameters under low-temperature (<150 °C) conditions on GSZO films and TFTs with bottom-gate configurations were examined. The contributions from this work are individually listed below.

1. Annealing temperature reduction from 250 °C to 140 °C tests showed degradation in electrical performance due to high density defects resulting in low quality film with poor semiconductor/insulator interface along with local atomic rearrangement with Sn^{2+} configuration being dominant.
2. Annealing duration tests (1, 6, 10 hours) showed improvement in device performance with increased annealing duration. SS reduces by half and μ_{FE} increases nearly 2 orders of magnitude from 1 hour annealed devices to 10 hour annealed devices. XPS shows an increase in Sn^{4+} with annealing duration which is known to improve device performance including μ_{FE} and is effective in annihilating only the shallow traps.
3. Increased deposition temperature (50 °C-100 °C) also showed improvement in device performance without the need for longer annealing durations. Devices deposited at 100 °C and annealed for 1 hour are comparable to devices deposited at 50 °C for 10 hours with an improved V_{ON}. An increase in Sn^{4+} at.% found in the bulk of the 100 °C film, likely causing an improvement in device performance since Sn^{4+} has the $[Kr](4d)^{10}(5s)^{0}$ electronic configuration needed to improve electron mobility.
4. When comparing low-temperature annealed devices to even higher temperature annealed devices (140 °C-450 °C), the 450 °C annealed device was superior in electrical

performance. The concentration of Sn^{4+} decreased from ~56 at.% to ~26 at.% with the decrease in the annealing temperature which explains one contributing factor towards degrading performance of the low annealed temperature device.

5. Reduction in the channel thickness (30 nm-10 nm) resulted in device improvement with V_{ON} improving (-14.5 V - -0.5 V), SS decreasing (2 V/dec - 1 V/dec) and mobility increasing (0.07 $cm^2/V \cdot s$ - 0.14 $cm^2/V \cdot s$). C-V data showed an improvement in performance with increased slope from depletion to accumulation region suggesting a decrease in defect density with decreasing channel thickness consistent with the improved I-V characteristics.

   RBS showed little change in compositional analysis with decreasing channel thickness however XRR showed film density to increase thus improving μ_{FE} and interface adhesion. Fully depleted channel is formed readily in the thinner film for small gate voltages thus leading to positive shift in V_{ON} and SS improvement. I_{ON} decreased nearly an order of magnitude after reducing the channel thickness from 30 nm to 10 nm due to the presence of interfacial electron traps which becomes more significant thus capturing more free carriers.

6. Lower temperature GSZO TFTs are strongly influenced by deposition parameters while higher temperature annealed films are not. This is due to the high density of O-related defects and Zn_I which become more prominent in low-temperature low-deposition pressure films.

7. GSZO films deposited at 10 mTorr were found to be more dense exhibiting smooth surfaces and interfaces as attested by AFM and XRR measurements with more than half in Sn4+ configuration as determined from XPS analysis. Hence these devices exhibited

better electrical performance with higher I_{ON}/I_{OFF} ratio and lower SS as compared to 1 mTorr device. These are dominated by oxygen vacancies which are filled forming a deep donor state as evidenced from I-V, C-V and stability measurements. Hence they were electrically stable but highly unstable under optical stress for shorter wavelengths of 550 nm and below. In contrast the 1mTorr background pressure deposited films were less dense, rough surface and interfaces, consisting of shallow oxygen vacancy and Zn_i states and high density of electron traps with Sn predominantly in the Sn^{2+} configuration. As a result the electrical performances were relatively poor and electrically instability being more severe than optically.

8. Bottom-gate **GSZO TFTs have been demonstrated on PEN substrates** which we believe **to be the first reported on these films**. Devices with planarization su-8 layer showed improvement in device performance when compared to devices without the su-8 layer likely the result of smoother gate oxide surface roughness. An $I_{ON/OFF}$ ~10^5, SS~0.7 V/dec and μ_{FE}~0.7 $cm^2/V \cdot s$ was achieved with the indium-free TAOS GSZO TFT on PEN. Poor thermal conductivity of the PEN was revealed in the abnormal output electrical characteristics for higher drain currents. These are preliminary data and there is considerable room for improvement in the fabrication of GSZO TFTs on PEN.

8.2 Overall Assessment

An understanding of the physics is important before making any device improvement, therefore in this work we have investigated the effects of different deposition parameters in order to better understand and manipulate the film properties. At low temperature annealing the oxygen vacancies, Zn interstitials and adsorption and desorption of oxygen play a dominant role and determines the location, density and nature of the states present in the band gap and the Sn

valency. This in turn determines the performance of the devices and the stability. It is also to be noted that the composition of the target that we have used is unique. The Sn and Ga atomic concentration is very low in comparison to those reported in literature. Also we have used only one target composition. In the case of IGZO the entire phase diagram was examined before the industry decided on the optimum value.

The focus of this work was to use the TFTs for flexible electronics and we have used very conservatively lower temperatures of 150 °C. One of the major problems is the removal of deep states. Any increase in the processing temperature would assist in significant reduction in the deep states. The plastic temperature has risen to 200 °C and this additional 50 °C is significant as one of our earlier work shows that deep states is significantly reduced on annealing at 250 °C.

Another problem is the presence of Sn^{2+} which we found lowers the mobility and higher SS. This study shows that we can manipulate this by deposition conditions. Higher oxygen pressure conditions facilitate Sn^{4+} however gives rise to deep states. With increased deposition pressure, annealing duration and annealing temperature comes considerable improvement in device performance. Hence even an increase in temperature by 50 C would potentially lead to further improvement in the device. Lastly the contacts. We have seen the contact and the post annealing contact is important and can improve the characteristics. Other tricks such as varying oxygen deposition pressure with thickness are other possibilities.

Overall GSZO has a very good potential to replace IGZO. We have not yet considered changing the target composition.

8.3 Future Work

Due to the sensitivity of fabricating bottom-gate GSZO TFTs on plastic, a careful examination of the fabrication process is fundamental to producing suitable electrical and optical performance, particularly the importance of fabricating devices in a timely manner due to the surface sensitivity of the GSZO film which is susceptible to compositional changes quickly over time. The addition of passivation layer(s) would greatly enhance the stability performance of devices both on n^+ Si and PEN. Hexamethyldisilazene (HMDS) is a probable option for passivation layer due to its fast formation through spinning however it is also recommended to explore PECVD deposited films such as SiO_2. Further exploration of defect states should be explored through an in-depth photo-excitation analysis on devices on PEN to compare to devices on n+ Si substrate. Greater control over compositional concentration is vital to improving the performance of the GSZO TFT regardless of the substrate. The addition of Sn in the target or a system with co-sputtering capabilities would allow the fine-tuning of film atomic concentration to improve device performance. The exploration of further increasing temperatures during the fabrication process such as the deposition temperature and PCA can possibly greatly enhance the devices. Finally a study of multi-layer channels deserve exploration due to the promising properties films deposited under different conditions may bring.

A completely separate area that can be explored are the novel 2D chalcogenides with potentially large carrier mobility replacing this family of oxide semiconductors as channel.

References

[1] Park, J.S., et al., *Review of recent developments in amorphous oxide semiconductor thin-film transistor devices.* Thin Solid Films, 2012. **520**(6): p. 1679-1693.

[2] Kim, D.H., et al., *Thickness Dependence of Gate Dielectric and Active Semiconductor on InGaZnO[sub 4] TFT Fabricated on Plastic Substrates.* Electrochemical and Solid-State Letters, 2008. **11**(12): p. H317.

[3] Chen, Y.-C., et al., *Bias-induced oxygen adsorption in zinc tin oxide thin film transistors under dynamic stress.* Applied Physics Letters, 2010. **96**(26): p. 262104.

[4] Jeong, Y., et al., *Bias Stress Stability of Solution-Processed Zinc Tin Oxide Thin-Film Transistors.* Journal of The Electrochemical Society, 2009. **156**(11): p. H808.

[5] Wikipedia, *World Production Trend.* Retrieved February 12, 2014.

[6] Kuo, Y.U., *Thin film transistors. 1. Amorphous silicon thin film transistors*. Kluwer Academic Publishers, 2004.

[7] Wager, J.F., et al., *An amorphous oxide semiconductor thin-film transistor route to oxide electronics.* Current Opinion in Solid State and Materials Science, 2013.

[8] Robertson, J., *Properties and doping limits of amorphous oxide semiconductors.* Journal of Non-Crystalline Solids, 2012. **358**(17): p. 2437-2442.

[9] Kenji N., Akihiro T., Toshio K., Masahiro H., Hideo H., *Room-temperature fabrication of transparent flexible thin film transistors using amorphous oxide semiconductors.* Nature, 2004. **432**: p. 5.

[10] Kamiya, T. and H. Hosono, *Material characteristics and applications of transparent amorphous oxide semiconductors.* NPG Asia Materials, 2010. **2**(1): p. 15-22.

[11] Fortunato, E.M.C., et al., *High mobility indium free amorphous oxide thin film transistors.* Applied Physics Letters, 2008. **92**(22): p. 222103.

[12] Ogo, Y., et al., *Amorphous Sn-Ga-Zn-O channel thin-film transistors.* physica status solidi (a), 2008. **205**(8): p. 1920-1924.

[13] Agency, J.S.a.T., *JST Signs Patent License Agreement with Samsung for High Performance TFT Technology.* 2011.

[14] Sharp, *IGZO Harmony Between Life and Technology http://www.sharpusa.com/ForHome/HomeEntertainment/LCDTV/igzo.aspx.2014*

[15] Fujitsu, *Fujitsu Lauches New Lineup of FMV Series PCs with Four New Models.* http://www.fujitsu.com/global/news/pr/archives/month/2013/20130605-01.html. 2013.

[16] LG, *LG Display Say UHD OLED TV Panel Products in Various Sizes and Designs in 2015.* http://flat-display-2.livedoor.biz/archives/28524794.html. 2013.

[17] Slivka, E., *Apple's iPad Air Adopts IGZO Technology for Thinner, Lower-Power Displays.* http://www.macrumors.com/2013/11/05/apples-ipad-air-adopts-igzo-technology-for-thinner-lower-power-displays/. 2013.

[18] Grumen, G. *Meet IGZO: The bleeding-edge LCD tech for the next iPhone*. Mobile Edge www.infoworld.com. 2013.

[19] Kim, D.-H., et al., *Sputter-deposited Ga-Sn-Zn-O thin films for transparent thin film transistors.* physica status solidi (a), 2011. **208**(12): p. 2934-2938.

[20] Kim, Y.J., et al., *Photobias instability of high performance solution processed amorphous zinc tin oxide transistors.* ACS Appl Mater Interfaces, 2013. **5**(8): p. 3255-61.

[21] Bradley, T., et al., *The effects of deposition conditions and annealing temperature on the performance of gallium tin zinc oxide thin film transistors.* 2013. **8626**: p. 862615-862615-10.

[22] Hosono, H., et al., *Factors controlling electron transport properties in transparent amorphous oxide semiconductors.* Journal of Non-Crystalline Solids, 2008. **354**(19-25): p. 2796-2800.

[23] Wu, J., et al., *Effect of active layer deposition temperature on the performance of sputtered amorphous In—Ga—Zn—O thin film transistors.* Journal of Semiconductors, 2014. **35**(1): p. 014003.

[24] Moon, M.R., et al., *The effects of a combined thermal treatment of substrate heating and post-annealing on the microstructure of InGaZnO films and the device performance of their thin film transistors.* Surface and Interface Analysis, 2012. **44**(11-12): p. 1431-1435.

[25] Se-I Oh, G.C., Hyunsang Hwang, Wu Lu and Jae Hyung, *Hydrogenated IGZO TFTs using High Pressure Hydrogen Annealing.* IEEE Trans. Electron Devices, 2013.

[26] Kim, D.-H., et al., *Effects of post-annealing on electrical properties of amorphous Ga-doped Zn–Sn–O semiconductor films.* Journal of Non-Crystalline Solids, 2012. **358**(18-19): p. 2616-2619.

[27] Chiang, H.Q., et al., *High mobility transparent thin-film transistors with amorphous zinc tin oxide channel layer.* Applied Physics Letters, 2005. **86**(1): p. 013503.

[28] Lee, J., et al., *The influence of the gate dielectrics on threshold voltage instability in amorphous indium-gallium-zinc oxide thin film transistors.* Applied Physics Letters, 2009. **95**(12): p. 123502.

[29] Se Yeob Park, J.H.s., Chang-Kyu Lee, Byeong Geun Son, Chul-Kyu Lee, Hyo Jin Kim, Rino Choi, Yu Jin Choi, Un Ki Kim, Cheol Seong Hwang, Hyeong Joon Kim, and Jae Kyeong Jeong, *Improvement in Photo-Bias Stability of High Mobility IZO TFTs by Oxygen High-Pressure Annealing.* IEEE Electron Device Letters, 2013. **34**(7): p. 804-806.

[30] Jeong, Y., et al., *Bias-stress-stable solution-processed oxide thin film transistors.* ACS Appl Mater Interfaces, 2010. **2**(3): p. 611-5.

[31] Aoi, T., et al., *DC sputter deposition of amorphous indium–gallium–zinc–oxide (a-IGZO) films with H2O introduction.* Thin Solid Films, 2010. **518**(11): p. 3004-3007.

[32] Barquinha, P., et al., *Toward High-Performance Amorphous GIZO TFTs.* Journal of The Electrochemical Society, 2009. **156**(3): p. H161.

[33] Jung, C.H., et al., *Transparent amorphous In–Ga–Zn–O thin film as function of various gas flows for TFT applications.* Thin Solid Films, 2009. **517**(14): p. 4078-4081.

[34] Chiang, H.Q., et al., *Processing effects on the stability of amorphous indium gallium zinc oxide thin-film transistors.* Journal of Non-Crystalline Solids, 2008. **354**(19-25): p. 2826-2830.

[35] Ding, X., et al., *Influence of the InGaZnO channel layer thickness on the performance of thin film transistors.* Superlattices and Microstructures, 2013. **63**: p. 70-78.

[36] Lim, S.J., S. Kwon, and H. Kim, *ZnO thin films prepared by atomic layer deposition and rf sputtering as an active layer for thin film transistor.* Thin Solid Films, 2008. **516**(7): p. 1523-1528.

[37] Lee, G.J., et al., *High performance, transparent a-IGZO TFTs on a flexible thin glass substrate.* Semiconductor Science and Technology, 2014. **29**(3): p. 035003.

[38] Jackson, W.B., R.L. Hoffman, and G.S. Herman, *High-performance flexible zinc tin oxide field-effect transistors.* Applied Physics Letters, 2005. **87**(19): p. 193503.

[39] Ito, M., et al., *Application of amorphous oxide TFT to electrophoretic display.* Journal of Non-Crystalline Solids, 2008. **354**(19-25): p. 2777-2782.

[40] K*urt Lesker PVD 75 E-Beam Evaporator. http://www.lesker.com/newweb/Vacuum_systems/deposition_systems_pvd_ProLinePVD75.cfm. Accessed February 25, 2014*

[41] Varian Cary 6000i UV-Vis-NIR Spectropohotometer *http://www.labwrench.com/?equipment.view/equipmentNo/4796/Varian/Cary-4000-5000-6000i/, As seen on February 25, 2014.*

[42] Bradley, T., *The Effects of Deposition Conditions on RF Sputtered Gallium Tin Zinc Oxide Thin Film Transistors.* 2012, Publshed Ph.D. North Carolina Agricultural & Technical State University, p. 134.

[43] I-Chung Chiu, I.-C.C., *Gate-Bias Stress Stability of P-Type SnO Thin Film Transistors Fabricated by RF-Sputtering.* IEEE Electron Device Letters, 2014. **35**(1).

[44] Kim, Y.-M., et al., *Investigation of zinc interstitial ions as the origin of anomalous stress-induced hump in amorphous indium gallium zinc oxide thin film transistors.* Applied Physics Letters, 2013. **102**(17): p. 173502.

[45] Kim, J.H., *Correlation of the change in transfer characteristics with the interfacial trap densities of amorphous In-Ga-Zn-O thin film transistors under light illumination.* Applied Physics Letters, 2011. **98**.

[46] Nayak, P.K., et al., *Impact of soft annealing on the performance of solution-processed amorphous zinc tin oxide thin-film transistors.* ACS Appl Mater Interfaces, 2013. **5**(9): p. 3587-90.

[47] Tsao, S.W., et al., *Hydrogen-induced improvements in electrical characteristics of a-IGZO thin-film transistors.* Solid-State Electronics, 2010. **54**(12): p. 1497-1499.

[48] Ogo, Y., et al., *Tin monoxide as an s-orbital-based p-type oxide semiconductor: Electronic structures and TFT application.* physica status solidi (a), 2009. **206**(9): p. 2187-2191.

[49] Chen, M., *X-ray photoelectron spectroscopy and auger electron spectroscopy studies of Al-doped ZnO films.* Applied Surface Science, 2000.

[50] Jeon, J.-W., et al., *Effect of annealing temperature on optical band-gap of amorphous indium zinc oxide film.* Journal of Alloys and Compounds, 2011. **509**(41): p. 10062-10065.

[51] Yabuta, H., et al., *High-mobility thin-film transistor with amorphous InGaZnO[sub 4] channel fabricated by room temperature rf-magnetron sputtering.* Applied Physics Letters, 2006. **89**(11): p. 112123.

[52] Chung, J.H., et al., *Effect of thickness of ZnO active layer on ZnO-TFT's characteristics.* Thin Solid Films, 2008. **516**(16): p. 5597-5601.

[53] Jeong, J.H., et al., *Origin of Subthreshold Swing Improvement in Amorphous Indium Gallium Zinc Oxide Transistors.* Electrochemical and Solid-State Letters, 2008. **11**(6): p. H157.

[54] Lee, M.-J., et al., *Device characteristics of amorphous In-Ga-Zn oxide thin-film transistors with varying channel thickness.* Semiconductor Science and Technology, 2013. **28**(12): p. 125014.

[55] Toshiaki Arai, H.I., *Annealing effects of anodized Al-based alloy for thin film transistors.* Thin Solid Films, 1998. **318**.

[56] T. Kawamura, H.U., S. Saito, H. Wakana, T. Mine, M. Hatano, K. Torii, T. Onai, *<1.5-V Operating Fully-Depleted Amorphous Oxide Thin Film Transistors.pdf>*.

[57] Raja, J., et al., *Enhancement of electrical stability of a-IGZO TFTs by improving the surface morphology and packing density of active channel.* Current Applied Physics, 2013. **13**(1): p. 246-251.

[58] Huang, X., et al., *Electrical instability of amorphous indium-gallium-zinc oxide thin film transistors under monochromatic light illumination.* Applied Physics Letters, 2012. **100**(24): p. 243505.

[59] Ji-Hoon Shin, D.-K.C., *Effect_of_oxygen_on_the_optical_and_the_electrical_properties_of_amorphous_InGaZnO_thin_films_prepared_by_RF_magnetron_sputtering.pdf.* Journal of the Korean Physical Society, 2008. **53**: p. 2019-2023.

[60] Jianke Y., N.X., Shaozhi D., Jun C., Juncong S., Han-Ping D. S., *Electrical and Photosensitive Characteristics of a-IGZO TFTs Related to Oxygen Vacancy.* IEEE Transactions on Electron Devices, 2011. **58**: p. 1121-1126.

[61] Seung Rim, Y., et al., *Defect reduction in photon-accelerated negative bias instability of InGaZnO thin-film transistors by high-pressure water vapor annealing.* Applied Physics Letters, 2013. **102**(14): p. 143503.

[62] McCall B., Alston R. and Iyer S., *A Study of Electrical and Optical Stability of GSZO Thin Film Transistors.* Unpublshed Ph.D. North Carolina Agricultural & Technical State University 2014.

[63] Qin, Y., et al., *Organic Thin-Film Transistors with Anodized Gate Dielectric Patterned by Self-Aligned Embossing on Flexible Substrates.* Advanced Functional Materials, 2012. **22**(6): p. 1209-1214.